# HV9931 Unity Power Factor LED Lamp Driver

## Introduction

Development of high-brightness light emitting diodes (LED) revolutionized the lighting industry in the recent years. Semiconductor light sources replace incandescent bulbs in an increasing number of applications due to their unsurpassed reliability and efficiency. Such applications include traffic signals, emergency lighting, hard-to-reach lighting fixtures, automotive lighting, accent and decorative lighting. Many of these applications demand off-line power drivers capable of regulated DC output current, low DC output voltage and input unity power factor.

A flyback converter can become a simple solution for these types of applications. When operating in discontinuous conduction mode, a flyback converter inherently provides a good power factor since the peak current in its inductor is proportional to the instantaneous input voltage. However, a very large electrolytic smoothing capacitor is needed at the load in order to attenuate the rectified AC line ripple component of the output current. Low dynamic resistance of LEDs aggravates the problem even further. There are power topologies that can resolve this problem by cascading converter stages using a single active switch. Most of these topologies include an input boost converter stage for shaping the input current. Hence they require a transformer with a high step-down turn ratio in order to drive low voltage LEDs. A power transformer would be needed even when galvanic isolation of the output in not required. Overall power efficiency, cost and reliability can be improved by using a step-down buck-boost input stage.

### Fig 1: Power conversion topology*

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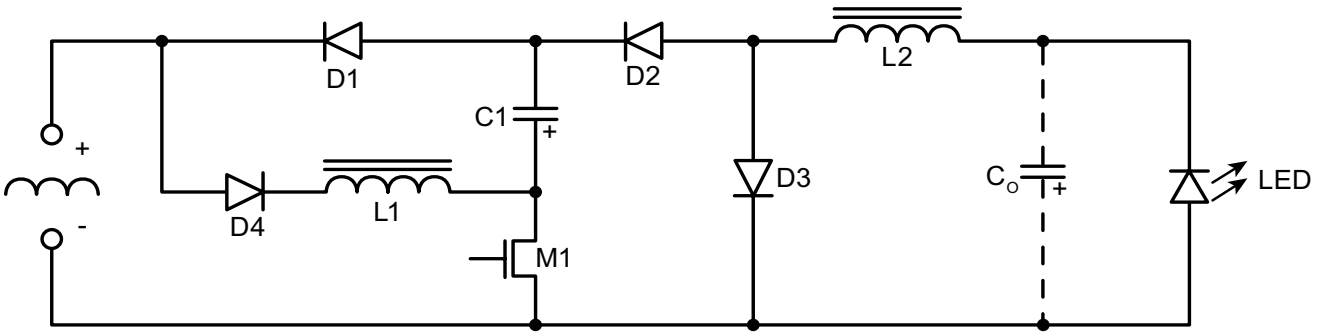
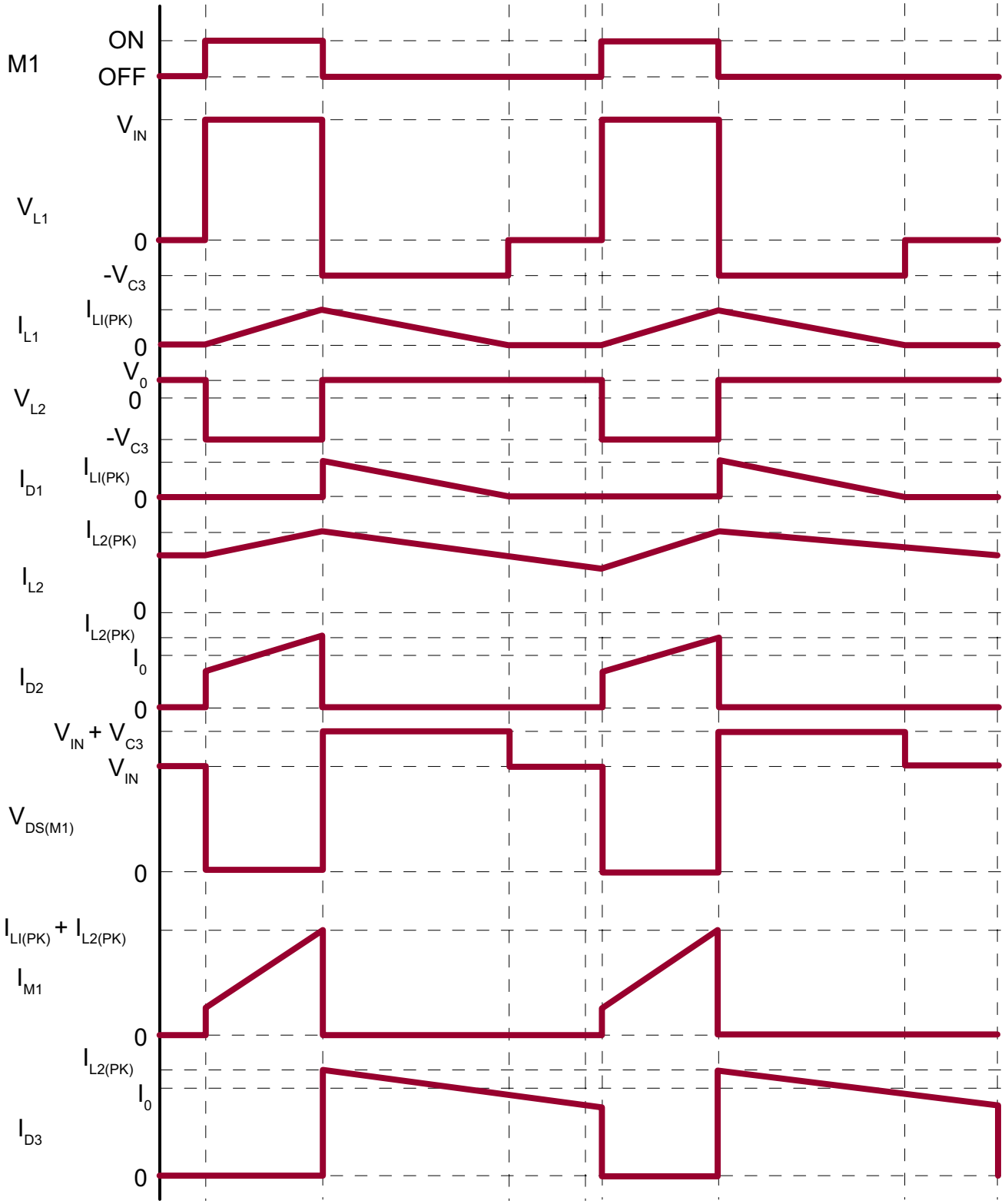



A simple transformerless power converter is shown in Fig.1. Its input buck-boost stage consisting of L1, C1, D1 and D4 is cascaded with an output buck stage including L2, D2, D3 and $C_O$. Both converter stages share a single power MOSFET M1. The input buck-boost stage operates in discontinuous conduction mode (DCM), while the output buck stage runs in continuous conduction mode (CCM). Both converter stages can operate as step-down voltage converters. The overall step-down ratio is a product of the step-down ratios of the two converter stages. Thus a high step-down ratio is achieved without using a transformer. Steady-state voltage and current waveforms of this converter are shown in Fig.2. Switching the MOSFET M1 on applies the rectified AC line voltage across L1. Current in L1 rises linearly. At the same time, the bulk capacitor C1 powers the output buck stage. (Note the negative polarity of the voltage across C1 with respect to ground when M1 is on.) The current in L2 ramps up. The current paths for this switching state are shown in Fig.3a.

When M1 turns off, D1 becomes forward-biased. The input inductor current diverts into C1. At the same time, the current in the output inductor L2 finds its way through D3. (See Fig. 3b.). The current in L1 ramps down. As soon as the current reaches zero, the diode D1 becomes reverse-biased and prevents the current in L1 from reversing. (The reverse current flow back into the input source would otherwise cause harmonic distortion of the input current and reduction in the overall efficiency.) Fig.3c depicts this switching state.

**Fig 2: Voltage and current switching waveforms**



The value of the bulk capacitor C1 needs to be large enough to attenuate rectified AC line ripple. Then the duty cycle D and the switching frequency $F_S$ can be assumed constant over the AC line cycle. In this case, both the peak current $I_{L1(PK)}$ in L1 and the average input current $I_{IN}$ are directly proportional to the input voltage $V_{IN}$. (See Fig. 4.) The factor $R_{eff} = 2 \cdot L1 \cdot F_S / D^2$ is the effective input resistance of the converter. This feature of the switching converter of Fig. 1 ensures low harmonic distortion of the input AC current and near-unity power factor. Other techniques using the HV9931 that can reduce harmonic distortion even further will be discussed below.

**Fig 3: Switching states of the converter:**
**(a) energizing L1 and L2, (b) de-energizing L1 and L2, (c) dead time of L1.**

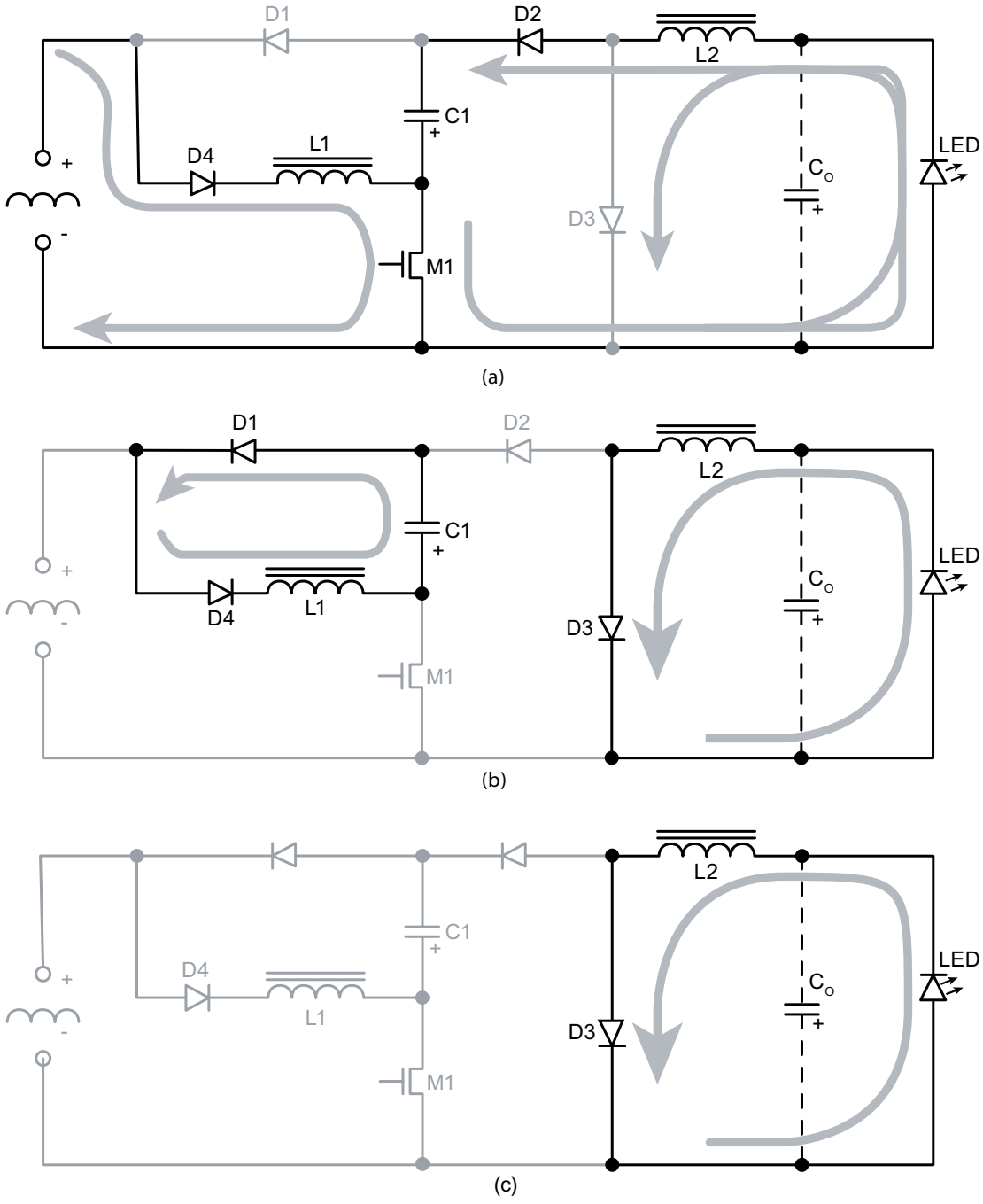
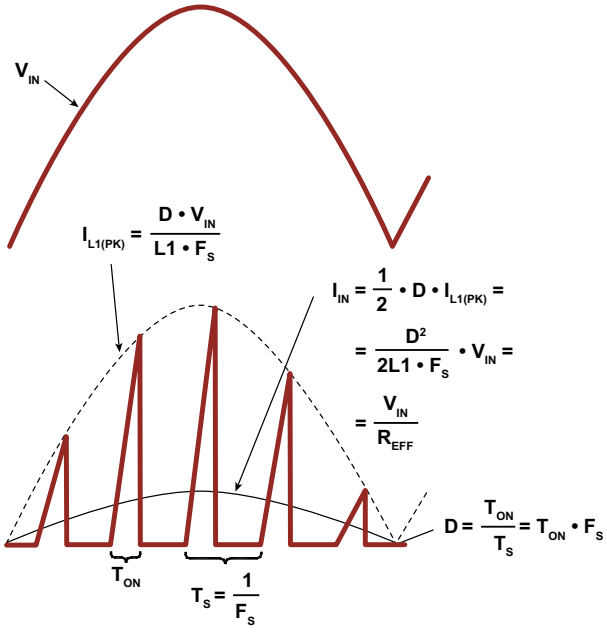


**Fig 4: Waveforms explaining the unity power factor feature of the HV9931.**




## LED Current Control Loop

The HV9931 is a peak current control IC that is specifically designed for optimally controlling the non-isolated single-stage PFC converter described above. A typical application circuit of the HV9931 is shown in Fig. 5.

Upon application of 12 - 450V at VIN, the built-in high voltage regulator circuit seeks to regulate 7.5V ± 5% at VDD. The circuit is equipped with an under-voltage protection comparator (UVLO) that inhibits switching until a threshold voltage is reached at VDD. A 0.5V hysteresis is included to prevent oscillation.

As soon the start-up threshold is reached at VDD, an internal oscillator circuit is enabled. The output signal of the oscillator triggers a PWM latch. The GATE output becomes high, the power MOSFET Q1 switches ON. The oscillator circuit can be programmed with a single resistor connected to RT for either constant switching frequency or fixed off-time operation. In the fixed off-time mode, the oscillator will set the PWM latch after a programmed time period following the turn-off of the GATE output. In order to program the HV9931 for constant frequency operation, the timing resistor needs to be connected between RT and GND. The switching frequency in this case can be calculated using the following equation:

$$F_S = \frac{1}{\alpha \bullet R_T + \tau_O} \quad (1)$$

where $\alpha$ = 40pF, $\tau_O$ = 880ns. Connecting the resistor from RT to GATE programs constant off-time:

$$T_{OFF} = \alpha \bullet R_T + \tau_O \quad (2)$$

It can be shown that the fixed off-time operating mode: a) reduces the voltage stress at C1; b) improves input AC ripple rejection; c) inherently introduces frequency jitter that can help reduce the size of the input EMI filter required. Hence, we will assume the fixed off-time mode for the purpose of this discussion.

The control circuit further includes two comparators for programming peak currents in L1 and L2. Both comparators use the ground potential (GND) as a reference and can be used to monitor voltage signals of negative polarity with respect to GND. A blanking delay of 215ns is added to prevent false tripping the comparators due to the circuit parasitics. The currents $i_{L1}$ and $i_{L2}$ that trip the comparators can be computed as:

$$i_{L(PK)} = \frac{V_{REF} \bullet R_{CS}}{R_{REF} \bullet R_S} \quad (3)$$

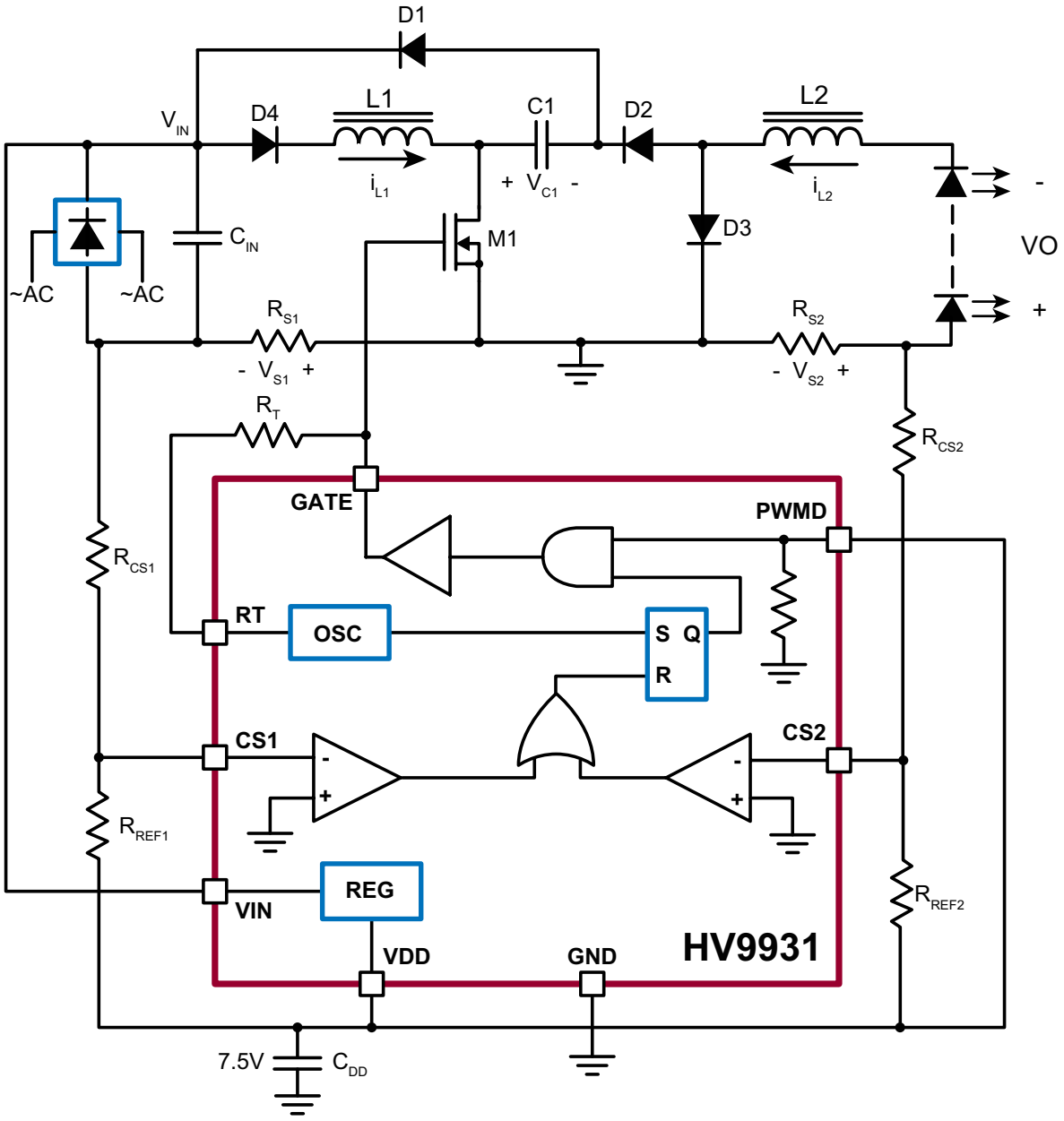
where $V_{REF}$ is an external reference voltage. We will use $V_{REF} = V_{DD}$ as an example. When either of the comparators detects negative input voltage at its CS input, the PWM latch resets, the GATE output becomes low, and the MOSFET Q1

turns off. Note, that since L2 is assumed to operate in CCM:

$$i_{L2(PK)} = i_{L2} + \frac{1}{2} \cdot \Delta i_{L2} \quad (4)$$

where $i_{L2}$ is the average current, and $\Delta i_{L2}$ is the peak-to-peak current ripple in L2. Thus the constant peak current control used in the HV9931 introduces a peak-to-average error $1/2\Delta i_{L2}$ that needs to be accounted for when programming the resistor divider $R_{REF2}/R_{CS2}$. Fortunately, this error is nearly constant for any input voltage at fixed $T_{OFF}$ and it is relatively small compared to $i_{L2}$ (15% typ.) Hence the ripple will have a minimal effect on the overall regulation of the output current. The error is however a function of the output voltage variation and the inductance value tolerances of L2.

**Fig 5: Typical HV9931 off-line PFC LED Driver application circuit**



## Power Converter Design

### Designing L1

We need to design the input buck-boost stage to operate in DCM for any given line and load condition to ensure low distortion of the input current and stability of the control loop. Therefore, let us assume that the current in L1 becomes critically continuous at full load and some minimum operating AC line voltage $V_{AC(MIN)}$. Naturally, this boundary conduction mode (BCM) condition occurs at the peak of each half-wave of the input AC current. If we assume a unity power factor (PF = 1), this boundary condition will then coincide with the peak input voltage $V_{AC(min)} \bullet \sqrt{2}$. Since both converter stages are in CCM, the ratio between the output and the input voltage can be expressed as:

$$\frac{V_O}{V_{AC(MIN)} \bullet \sqrt{2}} = \frac{D_{MAX} \bullet \eta_1}{1 - D_{MAX}} \bullet D_{MAX} \bullet \eta_2 = \frac{D^2_{MAX} \bullet \eta}{1 - D_{MAX}} \quad (5)$$

where $\eta_1$ and $\eta_2$ are the corresponding efficiencies of the input buck-boost stage and the output buck stage. The overall converter efficiency equals $\eta = \eta_1 \bullet \eta_2$. The duty ratio D of the switch M1 is the greatest at this condition. (Duty ratio is defined as $D = T_{ON} / T_S$, where $T_{ON}$ is the on-time of M1, and $T_S$ is the switching period.)

The input AC line current can be obtained from the output LED current $I_O$ and the output voltage $V_O$ as:

$$I_{AC} = \frac{V_O \bullet I_O}{V_{AC} \bullet \eta} \quad (6)$$

On the other hand,

$$I_{AC} \bullet \sqrt{2} = \frac{D}{2} \bullet I_{L1(PK)} \quad (7)$$

where the peak current $I_{L1(PK)}$ in L1 can be given as:

$$I_{L1(PK)} = \frac{V_{AC} \bullet \sqrt{2} \bullet T_{ON}}{L1} \quad (8)$$

Since our discussion is limited to the constant off-time case, let us express equation 8 in terms of $T_{OFF} = T_{ON} \bullet (1\text{-}D) / D$:

$$I_{L1(PK)} = \frac{V_{AC} \bullet \sqrt{2} \bullet T_{OFF}}{L1} \bullet \frac{D}{1 - D} \quad (9)$$

Finally, combining the equations (5), (6), (7) and (9) and solving for the inductance value gives:

$$L1 = \frac{V_{AC(MIN)} \bullet \sqrt{2} \bullet T_{OFF}}{4 \bullet I_O} \quad (10)$$

(Note, that the critical inductance L1 corresponding to the boundary conduction at $V_{AC(min)}$ and Io is independent of the output voltage or the efficiency of the converter.)

The designer must be careful when considering standard inductors for L1 or designing a custom one. Since L1 conducts discontinuous current, magnetic flux excursion in the core material can be quite significant. Hence the design of L1 is limited by the power dissipation in the magnetic core material rather than by the saturation current of the inductor selected.

### Designing C1

Selecting the capacitance value for C1 is based on the input harmonics limits required for a specific application. Lighting products are sold in large quantities, and thus these high volume products can potentially have a high impact on the low voltage public supply system. The European EN 61000-3-2 Class C limits are comparable to the limits imposed by ANSI C82.77 standards in the U.S. market, and restrict overall current harmonics to approximately 33%. Both the Class C and ANSI standards limit the 3rd harmonic current of lighting products to ~ 30%. The regulations for LED-based traffic signal heads are generally stricter and require total harmonic distortion (THD) to be less than 20% (ITE VTCSH Part 2).

The prevalent component of the AC ripple voltage across C1 is the 2nd AC line harmonic. This ripple causes modulation of the duty cycle according to:

$$D(t) = \frac{V_O}{\eta_2 \bullet V_C(t)} \quad (11)$$

where $V_C$ is voltage across C1. On the other hand, the input AC current can be expressed as:

$$I_{AC}(t) = \frac{V_{AC} \bullet \sqrt{2} \bullet D(t)^2 \bullet T_{OFF}}{2L1 \bullet (1 - D(t))} \bullet sin(2\pi \bullet F_{AC} \bullet t) \quad (12)$$

where $F_{AC}$ is the AC line frequency. Let us assume a small 2nd harmonics ripple voltage $v_C$ across C1, so that the voltage at C1 can be written as:

$$V_C(t) = V_C - v_C \bullet sin(4\pi \bullet F_{AC} \bullet t) \quad (13)$$

where $i_C << V_C$. Substituting (11) and (13) in (12) will produce a displaced fundamental term and a 3rd harmonic term in the AC line current. It can be shown from the resulting equation that the 3rd harmonic distortion of the input AC line current for a given relative 2nd harmonic ripple $K_C = i_C/V_C << 1$ is:

$$K_3 = \frac{\Delta I_{3rd}}{I_{AC}} \approx \frac{1}{2} \bullet \frac{2 - D}{1 - D} \bullet K_C \quad (14)$$

Thus every 1% of 2nd harmonic ripple at C1 will generate at least 1% of 3rd harmonic component in the AC line current even when the duty cycle is small.

Let us determine the capacitance value of C1 needed to limit the 3rd harmonic distortion to some given $K_3$. Equations (6), (7) and (9) together can be solved for the duty cycle D at any $V_{AC}$ within the operating range.

$$D = \frac{V_O \bullet I_O \bullet L1}{V^2_{AC} \bullet T_{OFF} \bullet \eta} \bullet \left( \sqrt{1 + \frac{V^2_{AC} \bullet T_{OFF} \bullet \eta}{V_O \bullet I_O \bullet L1}} - 1 \right)$$

Let us introduce a parameter δ as follows:

$$\delta = \frac{2 \bullet V^2_{AC} \bullet T_{OFF} \bullet \eta}{L1 \bullet V_O \bullet I_O} \quad (15)$$

Then the duty cycle can be expressed as:

$$D = \frac{2 \bullet (\sqrt{1 + \delta} - 1)}{\delta} \quad (16)$$

We can rewrite the equation (14) now as:

$$K_3 = K_C \bullet \frac{1}{1 - \frac{1}{\sqrt{1 + \delta}}} \quad (17)$$

Recalling that $D = V_O / (\eta_2 \bullet V_C)$ and using (16), we can determine the voltage at C1 for a given $V_{AC}$:

$$V_C = \frac{V_O}{2 \bullet \eta_2} \bullet (1 + \sqrt{1 + \delta}) \quad (18)$$

We have assumed that $K_C = i_C/V_C << 1$. This condition is met by selecting C1 large enough so that the AC ripple voltage at C1 is low. Therefore, C1 decouples the bulk of the AC ripple current at the output of the input converter stage. Averaged over a switching cycle, this current can be written as:

$$I_2(t) = \frac{V_{AC}(t) \bullet I_{AC}(t) \bullet \eta_1}{V_C} \quad (19)$$

where Vc is determined from (18). The AC line current $I_{AC}(t)$ is given by the equation (12). Then, under the assumptions made above, the AC component of $I_2(t)$ contains 2nd harmonic current only. This AC current in C1 can be expressed as:

$$I_C(t) = - \frac{D^2}{1 - D} \bullet \frac{\eta_1 \bullet V^2_{AC} \bullet T_{OFF}}{2 \bullet L1 \bullet V_C} \bullet cos(4\pi \bullet F_{AC} \bullet t) \quad (20)$$

Substituting D and $V_C$ from (16) and (18) gives:

$$I_C(t) = - \frac{2 \bullet I_O}{1 + \sqrt{1 + \delta}} \bullet cos(4\pi \bullet F_{AC} \bullet t) \quad (21)$$

Relative ripple voltage at C1 can be calculated as $K_C = I_{C(PK)} \bullet Z_C/V_C$, where $I_{C(PK)}$ is the amplitude of $I_C(t)$ and $Z_C = (4\pi \bullet F_{AC} \bullet C1)^{-1}$ is the impedance of C1 at $2 \bullet F_{AC}$. Substituting $V_C$ from (18), we obtain:

$$I_C(t) = \frac{1}{(1 + \sqrt{1 + \delta})^2} \bullet \frac{\eta_2 \bullet I_O}{\pi \bullet F_{AC} \bullet C1 \bullet V_O} \quad (22)$$

Solving the equation (22) for C1 and substituting $K_C$ from (17) we get:

$$C1 = \frac{1}{\delta \bullet \left[ 1 + \frac{1}{\sqrt{1 + \delta}} \right]} \frac{\eta_2 \bullet I_O}{\pi \bullet F_{AC} \bullet K_3 \bullet V_O} \quad (23)$$

The RMS value of the switching current in C1 can be calculated using the following equation:

$$I_{C(SW)} = I_O \bullet \sqrt{\frac{64}{9 \bullet \pi \bullet \eta \bullet \eta 1} \bullet \frac{V_O}{V_{AC} \bullet \sqrt{2}} + D} \qquad (23a)$$

The RMS value of the second AC line harmonic is derived from (21):

$$I_{C(LINE)} = \frac{I_O \bullet \sqrt{2}}{1 + \sqrt{1 + \delta}} \qquad (23b)$$

## Using Non-Electrolytic Capacitors for C1

The lifetime and the reliability of high brightness LEDs is remarkable. However, unlike incandescent light sources, LEDs generate conducted heat that needs to be dissipated within the lighting fixture. A power supply will be expected to function at elevated temperatures and match the lifetime of the LEDs when such power supply is integrated within the LED fixture. In many cases, this requirement rules out electrolytic capacitors commonly used in power supplies. As a “rule of thumb”, electrolytic capacitors suffer two times reduction of their life with every 10°C operating temperature rise. Therefore, it is desirable to be able to use a non-electrolytic capacitor for C1. Metallized polyester or PEN film capacitors can be considered for C1 as the most size and cost efficient replacement of aluminum electrolytic capacitors. However, they contribute a substantially higher cost per microfarad compared to electrolytic capacitors having similar voltage ratings. Thus, our design goal is to minimize the value of C1 while retaining low harmonic distortion.

As C1 becomes smaller, the condition of $K_C << 1$ is no longer met. Thus, we cannot use the equation (14) for calculating the 3rd harmonic distortion coefficient $K_3$. However, the equations (11) and (12) are still valid. We will combine these two equations and use $V_C(t) = V_C + \acute{\imath}_C(t)$, where $\acute{\imath}_C(t)$ is the AC ripple voltage at C1.

$$I_{AC}(t) = \frac{V_{AC} \bullet \sqrt{2} \bullet V_O^2 \bullet T_{OFF}}{2L1 \bullet \eta_2 \bullet (V_C + v_C(t))[(V_C + v_C(t)) \bullet \eta_2 - V_O]} \bullet \sin(2\pi \bullet F_{AC} \bullet t) \qquad (24)$$

We can see from the equation (24) that harmonic distortion of $I_{AC}(t)$ can be reduced by modulating $T_{OFF}$ as a function of $\acute{\imath}_C(t)$. In order to determine the modulation needed, we can expand the equation (24) in Taylor series in $\acute{\imath}_C(t)$. Then we can negate the 1st order term of the resulting expansion in $\acute{\imath}_C(t)$ by modulating $T_{OFF}$ inverse proportionally. This technique can achieve very good results since the linear term is responsible for the displaced fundamental and the bulk of 3rd harmonic in $I_{AC}(t)$.

One circuit implementation of this ripple cancellation feedback technique is shown in Fig.6. A charge pump circuit consisting of the capacitor $C_A$ and the diodes D5 and D6 performs level translation of $V_C$ to the ground potential. The voltage at C1 is reconstructed across the capacitor $C_B$. The values of $C_B$ and the bleeder resistor $R_B$ are selected such that $(2\pi R_B C_B)^{-1} >> 2 \bullet F_{AC}$ to preserve the ripple voltage $\acute{\imath}_C(t)$. Capacitor $C_{FF}$ decouples the DC component of $V_C$. The back-to-back connected Zener diodes D8 and D9 clamp the feedback voltage during initial charging of $C_{FF}$. A proportional AC current $\acute{\imath}_C(t)/R_{FF}$ then modulates the off-time programmed by the RT pin of the HV9931.

$$T_{OFF}(t) = \frac{\alpha \bullet (V_{RT} - V_D)}{\frac{V_{RT} - V_D}{R_T} - \frac{v_C(t)}{R_{FF}}} + \tau_O \qquad (25)$$

where $V_D = 0.7V$, $V_{RT} \approx 6.5V$. The capacitance value of $C_{FF}$ is selected such that $(2\pi R_{FF} C_{FF})^{-1} << 2 \bullet F_{AC}$. Substituting $T_{OFF}(t)$ given by (25) in the 1st order Taylor series term of the equation (24) and solving it for $R_{FF}$ gives the feedback resistor needed to cancel harmonic distortion of the input AC current.

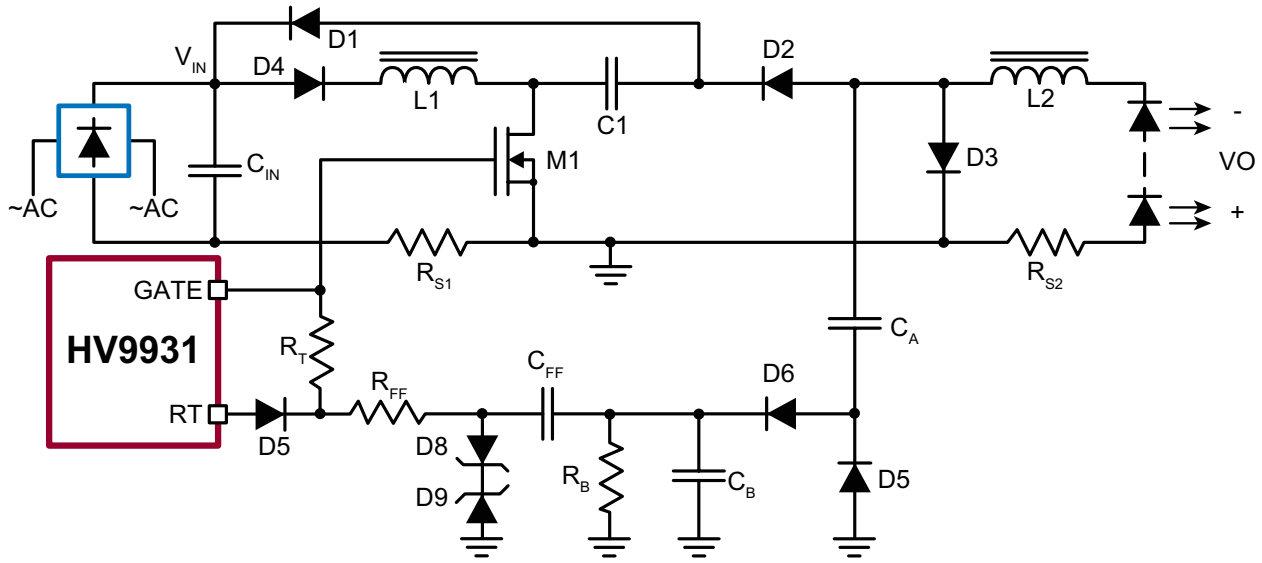
$$R_{FF} = \frac{\delta}{4 \bullet \sqrt{1 + \delta}} \bullet \frac{\alpha \bullet R_T^2 \bullet V_O}{\eta_2 \bullet (V_{RT} - V_D) \bullet (\alpha \bullet R_T + \tau_O)} \qquad (26)$$

(The derivation of the equation (26) has been omitted for the sake of simplicity.)

***Note, the circuit of Fig.6 contributes a positive feedback whose gain must not exceed the negative feedback gain imposed by the equation (11) to avoid loop oscillation!***

Therefore, perfect cancellation of harmonic distortion can only be achieved at a single point corresponding to the highest $V_O$ and $V_{AC}$. Thus, the equation (26) must use

**Fig 6: Feedback circuit improving the power factor and THD**




$V_{O(max)}$ and $V_{AC(max)}$. Nevertheless, a dramatic reduction of C1 can still be achieved (up to several times depending on the input AC voltage range required).The designer must not forget another constraint limiting the minimum value of C1. The voltage at C1 must not fall below the output voltage ($V_C > V_O$) in order to avoid interruptions of the output current.

$$K_{C(MAX)} < \frac{V_{C(MIN)} - V_O}{V_{C(MIN)}} \quad (27)$$

## Calculating L2

Calculating the value of the output filter inductor L2 is simple. The designer must decide on the amount of switching ripple current in L2. Then:

$$L2 = \frac{V_O \bullet T_{OFF}}{\Delta I_{L2} \bullet \eta_2} \quad (28)$$

where $\Delta I_{L2}$ is the peak-to-peak current ripple in L2. Larger values of L2 will produce smaller ripple $\Delta I_{L2}$, and therefore smaller peak-to-average error in the output current control loop. However, it would also make the output current sense comparator more susceptible to noise. It is a good practice to design L2 for $\Delta I_{L2}$ = 0.2~0.3. An output capacitor can be added to reduce the output ripple current further if needed.

Unlike the input inductor L1, design of L2 is typically limited by the saturation flux of its magnetic material. However, power dissipation due to the core loss may also need to be considered. The saturation current rating of the inductor must satisfy:

$$I_{SAT} > I_O + \frac{1}{2} \Delta I_{L2} \quad (29)$$

## Power Semiconductor Components

Let us calculate the voltage and the current ratings of the MOSFET M1 and the rectifiers D1-D4. The current in M1 is composed from the currents in the inductors L1 and L2. Hence, the RMS current in M1 can be computed as:

$$I_{D(M1)} = \sqrt{\frac{D_{MAX} \bullet I_{L1(PK)}^2}{6} + D_{MAX} I_O^2} \quad (30)$$

where $I_{L1(PK)}$ and $D_{max}$ are calculated from (9) and (16) at $V_{AC(min)}$. We disregarded the ripple current in L2 in the equation (30). The drain voltage rating of M1 can be determined as:

$$V_{DS(M1)} = V_{AC(MAX)} \sqrt{2} + V_{C(MAX)} (1 + K_C) \quad (31)$$

where $V_{C(max)}$ and $K_C$ are calculated at $V_{AC(max)}$ using (18) and (22). It is very important to find a good balance between the total gate charge Qg and the on resistance $R_{DS(ON)}$ of the power MOSFET M1. Using the MOSFET with lower $R_{DS(ON)}$ will not necessarily achieve greater efficiency. The HV9931 has a gate driving capability mainly limited by the power dissipation in the high voltage regulator. In addition to generating higher switching power loss, MOSFETs with high Qg will require more current from the regulator. Non-optimal selection of M1 may cause the HV9931 to overheat.

The highest currents in D1-D4 averaged over the AC line cycle can be calculated as:

$$I_{D1} = \frac{4 \bullet \sqrt{2}}{\pi} \bullet \frac{I_O}{\eta_1 \bullet (1 + \sqrt{1+ \delta_{MIN}})} \quad (32)$$

$$I_{D2} = D_{MAX} \bullet I_O = \frac{2 \bullet (\sqrt{1 + \delta_{MIN}} - 1)}{\delta_{MIN}} \bullet I_O \quad (33)$$

$$I_{D3} = (1 - D_{MIN}) \bullet I_O = \frac{(\sqrt{1 + \delta_{MAX}} - 1)^2}{\delta_{MIN}} \bullet I_O \quad (34)$$

$$I_{D4} = \frac{4 \bullet \sqrt{2}}{\pi} \bullet \left( \frac{2 \bullet \sqrt{2}}{\delta_{MIN}} + \frac{1}{\eta_1 \bullet (1 + \sqrt{1+ \delta_{MIN}})} \right) \bullet I_O \quad (35)$$

where $\delta_{MAX}$ and $\delta_{MIN}$ are calculated from (15) at $V_{AC(MAX)}$ and $V_{AC(MIN)}$ correspondingly. Peak currents in D1 and D4 equal to $I_{L1(PK)}$ determined from (9) at $V_{AC(MIN)}$. Peak currents in D2 and D3 are computed as $I_O + ½\Delta I_{L2}$. The voltage ratings for D1-D3 are given as:

$$V_{R(D1)} = V_{AC(MAX)} \sqrt{2} + V_C(1 + K_C) \quad (36)$$

$$V_{R(D2)} = V_{AC(MAX)} \sqrt{2} \quad (37)$$

$$V_{R(D3)} = V_C (1 + K_C) \quad (38)$$

where $V_C$ and $K_C$ are calculated at $V_{AC(MAX)}$ from the equations (18) and (22).

The required reverse voltage rating of D4 depends on several factors. The dead time switching state of Fig.3(c) is characterized by a post-conduction resonance. The LC tank is formed by L1 and the parasitic capacitance of D1, D4 and M1. The resonant period can be estimated as:

$$T_R = 2\pi \sqrt{\frac{L_1 \bullet C_{j4}(C_{OSS} + C_{j1})}{C_{OSS} + C_{j1} + C_{j4}}} \quad (39)$$

where $C_{OSS}$ is the output capacitance of M1, $C_{j1}$ and $C_{j4}$ are reverse-biased junction capacitances of D1 and D4 correspondingly. Due to a finite reverse recovery time of D1, the input inductor L1 develops certain reverse current in the beginning of the dead time. Since L1 runs in DCM, reverse recovery of D1 is negligible from the overall power efficiency standpoint. However, even a small reverse current in L1 can cause a very high voltage spike across D4 when both diodes stop conducting. Thus, ultra fast recovery rectifier is recommended for D1.

Since $C_{j4} << C_{OSS}$ typically, the post-conduction oscillation occurs mainly across D4. The drain voltage of M1 will remain almost unchanged throughout the dead time. Besides causing the high voltage stress across D4, this oscillation may affect the EMI performance of the circuit. Thus, adding an RC snubber circuit across D4 is recommended. If the snubber capacitance value is greater than ($C_{OSS}$+$C_{j1}$), the reverse voltage rating of D4 can be reduced significantly. A fast 400V rectifier can be used for D4 in a universal 90-260VAC LED driver with adequate selection of the RC snubber components.

Using ultra-fast recovery rectifiers for D2 and D3 is essential for good efficiency of the LED driver. Both diodes operate at high current and are subjected to fast transitions and high reverse voltage.

## PWM And Linear Dimming

Many LED applications require dimming. Two types of dimming are available: analog and PWM. With analog (or linear) dimming, 50% brightness is achieved by applying 50% of the maximum current to the LED. Drawbacks to this method include LED color shift and the need for an analog control signal, which is not sometimes readily available. PWM dimming is achieved by applying full current to the LED at a reduced duty cycle. For 50% brightness, full current is applied at a 50% duty cycle. The frequency of the PWM signal must be above 100 Hz to ensure that the PWM pulsing is not visible to the human eye. The maximum PWM frequency depends upon the power-supply startup and response times. The HV9931 features a PWMD enable input that accepts a PWM dimming control logic signal. The GATE output is disabled when this signal is low. At the same time, since M1 is off and the rectifier D4 is reverse biased there is no discharge path for C1. Hence the current in L2 will recover within a single switching cycle back to its original level with no overshoots as soon as the PWMD signal becomes high again.

In some cases, however, linear dimming is preferred for simplicity and component count reduction when the PWM control signal is not available. On the first glance at the HV9931, merely programming the divider ratio of $R_{REF2}$ and $R_{CS2}$ can control the output LED current proportionally. However, this method would affect the required voltage ratings of C1, M1 and D1-D4. The problem can be explained by the power imbalance between the input DCM and the output CCM converter stages. The DC voltage conversion ratio of the output buck stage is given by (11). Hence the duty cycle of the CCM buck stage is independent of the output current. On the other hand, the input buck-boost stage delivers an amount of energy every switching cycle that is a function of the duty ratio and the switching frequency. The balance is achieved by increased voltage at C1 for smaller output currents. The voltage stress can be very significant for universal 90 - 260VAC input designs.

Fig.7 shows $V_C$ as a function of the output current based on the equation (18) for the universal LED driver given in the Design Example section of this application note. (Note that $V_C$ exhibits no further increase as the output buck stage enters DCM.) Thus, the linear dimming method will require significantly higher voltage ratings of the switching components.

The voltage stress problem at light load can be resolved by making $T_{OFF}$ proportional to $I_O$. The equation (18) will no longer be load dependent since $\delta$ = const when $T_{OFF}/I_O$ = const. One possible implementation of this dimming technique is depicted in Fig. 8. The timing resistor is altered in proportion with the output divider ratio. In order to maintain constant $V_C$, the resistor values must satisfy:

$$\frac{R_a}{R_{CS2}} = \frac{R_b}{R_T} \qquad (40)$$

However, the designer must be careful when using this technique, since, for example, linear dimming to 33% of the nominal load will cause the switching frequency of the converter to triple.

**Fig 7. Voltage at C1 as a function of the output current in the case of linear dimming.**

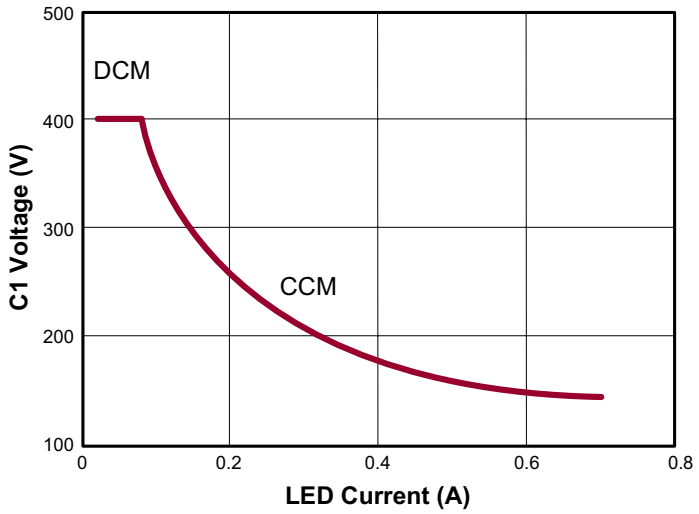
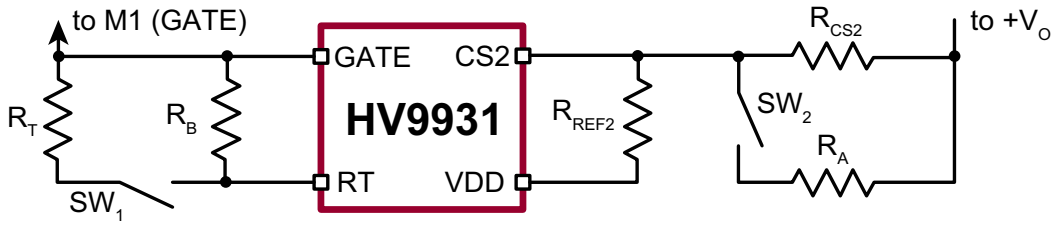



**Fig 8. Linear dimming circuit maintaining constant voltage at C1**



## Phase-Control Dimming

One of the main advantages of the HV9931 LED driver solution is its inherent compatibility with phase-control dimmers. Solid-state light dimmers have been around since the 1960's. They work by varying the duty cycle of the full AC voltage that is applied to the lights being controlled. Typical light dimmers are built using thyristors, and the exact time when the thyristor is triggered is relative to the zero crossings of the AC power. When the thyristor is triggered it keeps conducting until the current passing though it goes to zero.

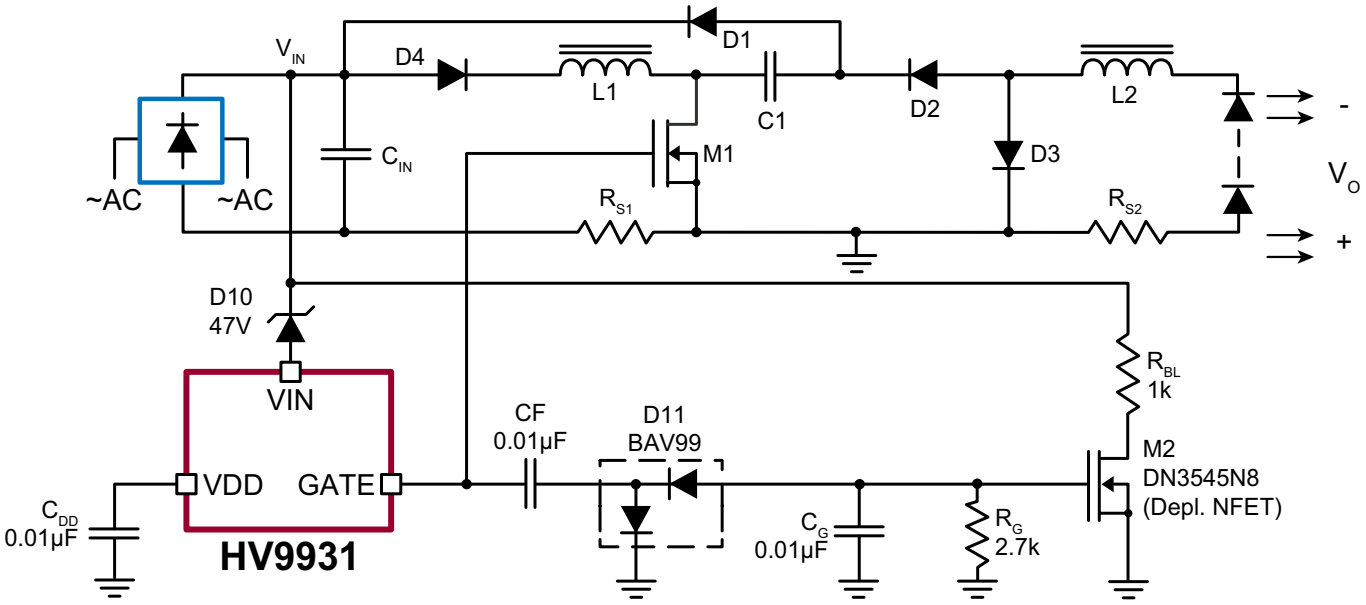
Typical switch-mode LED drivers do not work well with phase-control dimmers because of the large output capacitance that they must use to filter the 2nd AC line harmonic ripple. Interruptions of the voltage at the output of a phase dimmer would have no effect on the output current of these LED drivers.

The HV9931 LED driver cuts the output current naturally as soon as its GATE output switching halts. The energy stored in C1 is preserved until the switching resumes. Merely selecting a $V_{DD}$ bypass capacitor $C_{DD}$ small enough (about 0.1µF typically) will disable the HV9931 switching when the input AC line voltage drops out. Adding a Zener diode in series with $V_{IN}$ ($V_Z \approx 50V$ for 120VAC) is recommended for reliable phase-control operation and under-voltage protection. Alternatively, the PWMD pin can be used to disable switching when the input voltage is low.

However, some additional circuitry may be needed depending on the topology and the power ratings of the phase-control dimmer or in order to make the HV9931 work with any dimmer. Most dimmers include an EMI filter for attenuating RF interference caused by the thyristor switching. A typical 2-wire 600W dimmer is shunted by a 0.047~0.1µF capacitor that causes substantial AC leakage current. This current can develop significant voltage at the input of the LED driver while it is off. Hence multiple premature startup attempts may occur causing the LEDs to flicker. In order to resolve this problem, a bleeder resistor can be connected across the LED driver input while the HV9931 is off. The resistor can be disconnected from the input as soon as the HV9931 resumes switching. The circuit diagram of Fig. 9 shows one simple implementation of this technique.Inrush charging of the capacitance at the AC input of the LED driver needs to be considered also. The thyristor may turn off due to a zero-current condition created by a resonance in the LC circuit formed by the filter inductor of the dimmer (a few tens of µH typically) and the input capacitance of the LED driver. Although $R_{BL}$ will help to damp this resonance, an additional resistor may be needed in series with the AC input of the LED driver.

Input power consumption of the LED driver needs to be taken into account too. Lower power LED drivers (10W or less) may draw input current that is smaller than the holding current of the thyristors. Use phase-control dimmers having the adequate power ratings, or connect more than one LED driver to the dimmer output to avoid this problem.

**Fig 9. Bleeder circuit for use with 120VAC phase-control dimmers**



## Output Open Circuit And Input Under Voltage Protection

HV9931 is a constant output current source. Hence it can generate destructive voltage at its output in the case of an output open circuit condition. A simple circuit shown in Fig. 10 protects the HV9931 LED driver from the output over-voltage. Zener voltage of D12 greater than the maximum output voltage must be selected. Resistor $R_{OV}$ is typically 100~200Ω. However, it still may affects the output current divider ratio and needs to be included in the calculations by replacing $R_{CS2}$ by ($R_{CS2}$ + $R_{OV}$) in the equation (3). Note, that the open circuit can create an over-voltage condition across C1. This voltage stress can be limited by connecting a Zener diode or TVS across C1 limiting the voltage to some acceptable level greater than $V_{C(max)}$. The power dissipation in this voltage clamp device is usually small, since the HV9931 operates at minimum duty cycle during the open circuit condition.

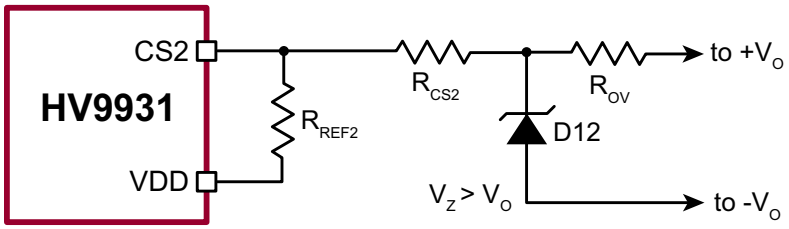
The HV9931 inherently protects the LED driver from an input under voltage condition by limiting the input current. However, increased input current may generate excessive power dissipation in L1, D4, M1 and $R_{CS1}$. Additional protection is recommended by connecting a Zener diode in series with the $V_{IN}$ pin of the HV9931. (See D10 in Fig. 9)

In addition to D10, an improved input under voltage protection circuit is shown in Fig.10a that can achieve better performance compared to the simple fixed input current limiting. The reference for the CS1 comparator is derived from the input rectified AC waveform. The voltage divider ratio of $R_1$ :$R_{REF1}$ is programmed such that the Zener diode $Z_{REF1}$ clamps the divider voltage at any input greater than $V_{AC(min)}$, i.e.:

$$R_1 = R_{REF1} \bullet \frac{V_{AC(MIN)} \bullet \sqrt{2} - V_{ZREF1}}{V_{ZREF1}} \qquad (41)$$

$V_{REF}$ = $V_{ZREF1}$ should be used with the equation (3) to set the peak current limit for L1 within the normal operating input AC voltage range. When the input voltage falls below $V_{AC(min)}$, the reference voltage will reduce too preventing the inductor L1 from entering continuous conduction mode (CCM). (Operating L1 in CCM can cause undesirable LED flickering, audible noise and excessive heat dissipation due to the loop oscillation.) $R_{BIAS}$ creates a positive offset voltage to maintain the reference above 0V in the zero crossings of the AC line voltage, and thereby prevents interruptions of the output current.

### Fig 10. Output open circuit protection




### Fig 10a. Input under voltage protection

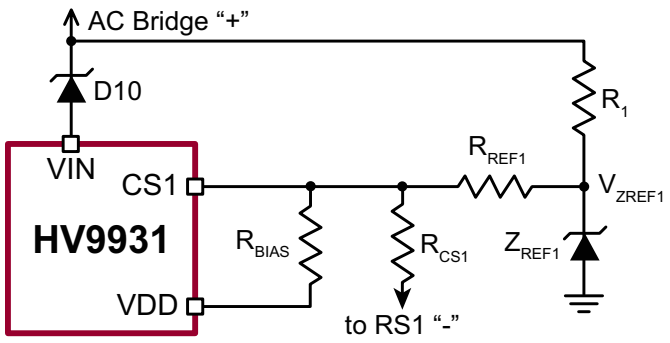
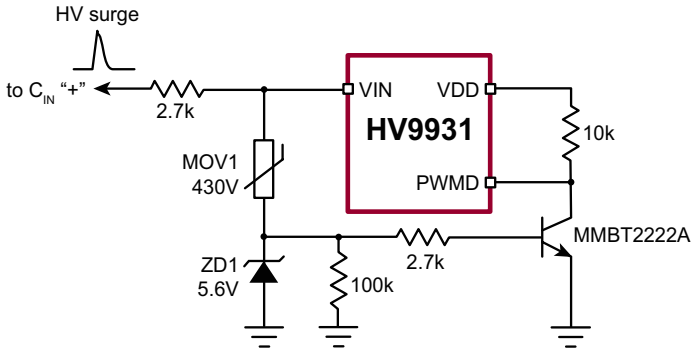


**Fig 11. Transient voltage protection.**




## Surge Immunity and EMI Considerations

High voltage surges occur on the AC power mains as a result of switching operations in the power grid and from nearby lightning strikes. LED lighting and signal equipment may be subjected to surge immunity compliance testing in accordance with various standards (EN61000-4-5, NEMA TS-2 2.1.8 etc.) to insure its continued reliable operation if subjected to realistic levels of surge voltages. The HV9931 LED driver circuit relies mainly on the transient suppressors (MOV, TVS) to protect it from the input AC line surge. There is little capacitance available at the AC input of the LED driver to absorb high surge energy. Thus a transient suppressor needs to be connected across the AC input terminals.

Additional protection circuitry may be also required to protect M1, D1, D2 and the HV9931 itself. A simple circuit shown in Fig.11 clamps the voltage at VIN in the case of an input over-voltage transient. At the same time, it disables the GATE output of the HV9931 to protect the switching components. When HV9931 is disabled, M1 and D1 will only have to withstand the input surge voltage $V_{SURGE}$ rather than ($V_{SURGE}$ + $V_C$).

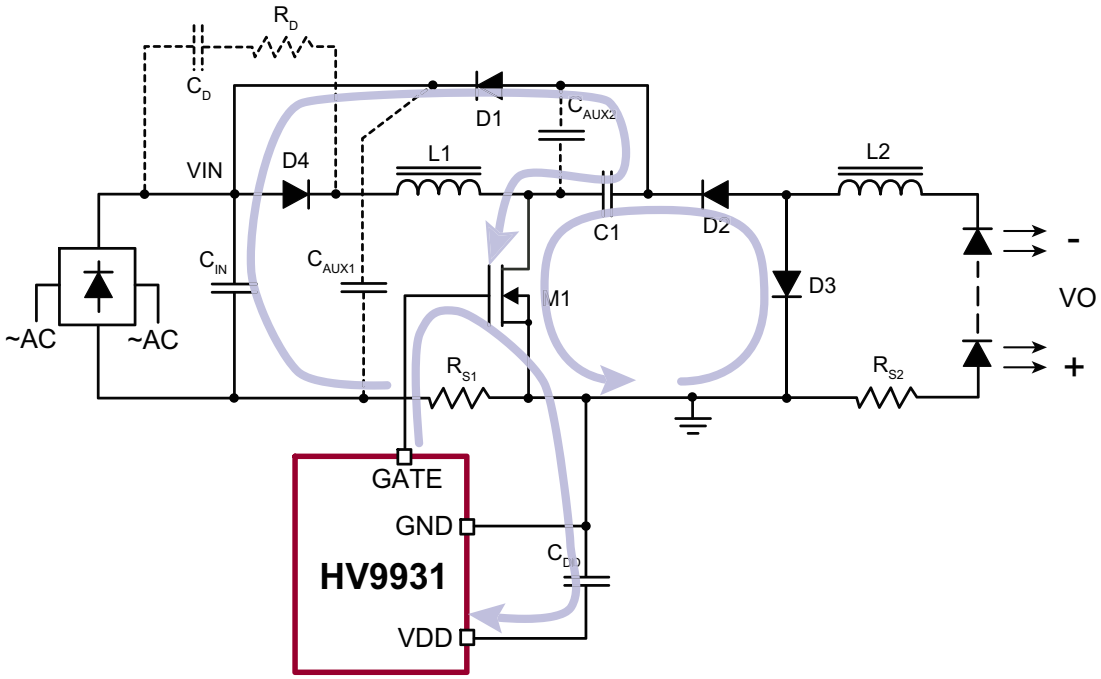
As with all switching converters, selection of the input filter is critical to obtaining good EMI. The HV9931 solution provides an inherent advantage of the frequency dither due to the AC voltage ripple across C1 when the fixed off-time operating mode is used. The C1 voltage feedback introduces additional frequency dither when utilized. Hence the required noise attenuation can be lowered yielding a smaller EMI filter.

Some important guidelines must be followed for optimal EMI performance of the HV9931 power converter. The area of the fast switching loops shown in Fig.11 must be minimized. The first loop including of M1, C1, D2 and D3 can significantly degrade the overall EMI performance due to the reverse recovery current in D3. Using soft recovery diode is recommended for D3. Adding an RC snubber circuit across D3 can be useful (not shown in Fig.11). The second loop consists of $C_{IN}$, D1, C1, M1 and $R_{S1}$. Since the input buck-boost stage runs in DCM, the reverse recovery current in D1 is insignificant. However, charging its junction capacitance can generate fast current transients. The large physical dimensions of C1 can complicate optimal routing of these loops. Auxiliary low ESR/ESL capacitors $C_{aux1}$ and $C_{aux2}$ can be used for optimizing the printed circuit board routing. $C_{aux1}$ and $C_{aux2}$ are responsible for the fast switching transition currents only and hence are typically very small. When these bypass capacitors are used, the areas formed by $C_{aux1}$, D1, $C_{aux2}$, M1, $R_{S1}$ and M1, $C_{aux2}$, D2, D3 need to be considered mainly.

Optimal routing of the HV9931 gate output loop can be important for EMI performance as well as for preventing destructive oscillations of the M1 gate voltage. The gate driver loop area must be minimized. The trace connecting the source terminal of M1 with the GND pin of the HV9931 must be as short as possible. The $V_{DD}$ bypass capacitor $C_{DD}$ must have low ESR and needs to be placed in the immediate proximity of the HV9931.

Post-conduction oscillation across D4 during the dead time of L1 can be another substantial source of RF emission. Adding a snubber circuit ($R_d$ and $C_d$ in Fig.11) can help significantly. In addition, this snubber is needed to reduce the voltage stress at D4 as it has been discussed in the previous sections.

**Fig 12. Fast switching current loops.**




**LED DRIVER DESIGN EXAMPLE**

Let us design a power converter for driving LEDs with the following characteristics:

| | |
|---|---|
| Input AC Line Voltage | 80 - 260VAC, 50-60Hz |
| Output Current | 750mA |
| Output Current Ripple | ±15% |
| Output Voltage | 25V (max.) |
| THD | <20% at 120VAC |
| OFF Time | 10µs |
| Predicted Efficiency | 76% |

We will assume that the efficiencies of the input buck-boost stage and the output buck stage are $\eta_1 = 0.85$ and $\eta_2 = 0.9$ correspondingly. The efficiency of a DCM buck-boost stage is typically lower compared to the CCM buck stage. The overall efficiency $\eta = \eta_1\eta_2 \approx 0.76$.

**Step 1.** Using the equation (2), we will calculate the timing resistor $R_T$ value for $T_{OFF}$ = 10µs. The resulting timing resistor:

$$R_T = 228K.$$

**Step 2.** We will allow 30% peak-to-peak switching current ripple in L2, or $\Delta i_{L2} = 0.3 i_{L2} = 0.225A$. Then according to the equation (4), the peak current in L2 is:

$$i_{L2(PK)} = 0.86A.$$

The value of L2 can be calculated from the equation (28).

$$L2 \approx 1.2mH$$

The DC current rating of L2 equals to $I_O$ = 0.75A. The saturation current must satisfy the condition (29) resulting in $I_{SAT} > 0.86A$.

**Step 3.** Assuming 0.25W power dissipation in the output current sense resistor $R_{S2}$, we can calculate its value.

$$R_{S2} = \frac{0.25W}{I_O^2} \approx 0.44\Omega$$

We will select a 0.47Ω 1/2W resistor for $R_{S2}$. Let us use the $V_{DD}$ pin as a reference voltage ($V_{DD}$ = 7.5V).

(Note, that although $V_{DD}$ is relatively precise, it may exhibit certain dropouts near the AC line voltage cusps when there is no input voltage available at $V_{IN}$. An external voltage reference is needed for better accuracy.) Selecting $R_{REF2}$ = 100K, we can calculate the value of $R_{CS2}$ using the equation (3).

$$R_{CS2} = 5.4K\Omega$$

**Step 4.** The input inductor L1 is assumed to reach boundary conduction mode (BCM) at $V_{AC(MIN)}$ at the peak of the input voltage hump. Using the equation (10), we can calculate the critical inductance value that meets this condition.

$$L1 = 377\mu H$$

**Step 5.** Let us calculate the parameter δ and the duty cycle D at $V_{AC(MIN)}$, $V_{AC(MAX)}$ and $V_{AC}$ using equations (15) and (16):

1) $\delta_{min}$ = 14, $D_{max}$ = 0.41 at 80VAC;
2) $\delta_{max}$ = 146, $D_{min}$ = 0.15 at 260VAC;
3) δ = 31, D = 0.3 at 120VAC.

**Step 6.** The maximum peak current in L1 will occur at $V_{AC(min)}$. It can be calculated from the equation (9).

$$i_{L1(PK)} = 2.1A$$

Note that most “off-the-shelf” 330µH DC chokes may be not suitable for L1. Since the current in L1 cycles from 0 to as high as $i_{L1(PK)}$ every switching cycle, there may be excessive power dissipated in the magnetic core of L1 due to large magnetic flux excursion. On the other hand, the wire gauge used in such inductors is selected based on its DC current rating, whereas the RMS current in L1 is substantially lower than its peak current. Thus, custom designing of L1 is likely to produce a more size efficient solution.

**Step 7.** The next step is calculating the input current sense and divider resistors $R_{S1}$ and $R_{CS1}$. Let us allow 0.1W of power dissipation in $R_{S1}$ at $V_{AC(MIN)}$. Power dissipation in $R_{S1}$ can be calculated as:

$$W_{RS1} = \frac{D_{MAX} \bullet I_{L1(PK)}^2 \bullet R_{S1}}{6}$$

Solving this equation for $R_{S1}$, we obtain:

$$R_{S1} \approx 0.47\Omega$$

Let us select $R_{S1}$ 0.47Ω 1/4W. To calculate $R_{CS1}$, we will use the equation (3) assuming $V_{REF} = V_{DD}$ and $R_{REF1}$ = 100K as before. We will program the peak input current limit as 120% of $i_{L1(PK)}$. Then:

$$R_{CS1} = 15.8K\Omega$$

**Step 8.** Let us assume the third harmonic distortion coefficient $K_3$ = 0.15 at $V_{AC}$ = 120VAC. Then, the equation (23) gives the value of C1.

$$C1 \approx 31\mu F$$

Using the same equations (18) at $V_{AC}$ = 260VAC, we can calculate the required voltage rating of C1.

$$V_{C(MAX)} = 182V$$

The voltage ripple at C1 is small at high input voltage. The equation (22) gives $K_{C(MIN)}$ = 0.032. Thus, the peak voltage at C1 is:

$$V_{C(PK)} = (1 + K_{C(MIN)})\, V_{C(MAX)} = 188V$$

The switching ripple current rating is calculated using the equations (23a):

$I_{C(sw)(MAX)} = 0.82A(rms)$ at 80VAC,
$I_{C(sw)} = 0.68A(rms)$ at 120VAC.

The 120Hz ripple current rating is calculated using the equations (23b):

$I_{C(LINE)(MAX)} = 0.22A(rms)$ at 80VAC,
$I_{C(LINE)} = 0.16A(rms)$ at 120VAC.

An electrolytic capacitor 33uF,200V can be selected for C1.

**Step 9.** If a smaller film capacitor is desired for C1, the circuit of **Figure 6** can be used. The value of $R_{FF}$ is calculated at $V_{AC} = V_{AC(MAX)} = 260VAC$ and $V_O = V_{O(MAX)} = 25V$ using the equation (26).

$$R_{FF} = 3M\Omega$$

Select $R_{FF}$ 3.3MΩ to avoid loop oscillation at high AC line voltage. $C_{FF}$ is selected such that:

$$C_{FF} >> \frac{1}{2\pi \bullet R_{FF} \bullet 100Hz}$$

Select $C_{FF}$ 4.7nF, 200V. The minimum value of C1 is limited by (27). Calculation of the C1 value needed to meet the desired harmonic distortion of $I_{AC}$ is very complex. The designer may want to experiment with different capacitance values of C1 to find the optimal one. Experimental verification shows, however, that THD<20% at 120VAC is possible with less than 1/3 of the C1 value calculated above. Two 4.7uF 250V metalized polyester film capacitors connected in parallel were used.

The $R_B$ value is selected based on the desired power dissipation such that $R_B << R_{FF}$. A 330K resistor will dissipate 0.1W at $V_{C(max)} = 182V$. The value of $C_B$ is calculated from:

$$C_B >> \frac{1}{2\pi \bullet R_B \bullet 120Hz} \approx 4.0nF$$

The flying capacitor $C_A$ must be selected such that:

$$C_A >> \frac{T_{OFF}}{R_B} \approx 25pF$$

We can select $C_B = C_A = 4700pF$ for simplicity. Both capacitors must be rated to withstand $V_{C(pk)}$. Zener diodes D8 and D9 must not distort the AC ripple waveform at the output of $C_{FF}$. In other words, their breakdown voltage must be set higher than the C1 voltage ripple amplitude at 120VAC. Leaving D8 and D9 out or selecting the diodes with excessively high breakdown voltage may increase the start-up time of the LED driver.

**Step 10.** Optimal selecting of the switching MOSFET M1 is based on finding a good balance between the total gate charge $Q_g$ and the on-resistance $R_{DS(ON)}$. The drain voltage rating is given by the equation (31).

$$V_{DS(max)} = 556V$$

Acceptable $Q_g$ is limited by the allowed power dissipation in the HV9931. The power dissipation can be estimated as:

$$W_{REG(max)} = \left( \frac{2\sqrt{2}}{\pi} \bullet V_{AC(max)} - V_Z \right) \bullet \left( \frac{Q_g \bullet (1 - D_{min})}{T_{OFF}} + \frac{V_{REF}}{R_{REF1}} + \frac{V_{REF}}{R_{REF2}} + 1mA \right)$$

where $V_Z$ is Zener voltage of D10.

Let us select SPP03N60C3 for M1. This is a 650V, 3.2A MOSFET by Infineon Technologies with $R_{DS(ON)}$ = 1.26Ω and $Q_{g(max)} \approx 13nC$ at $V_{DS} = 420V$, $V_{GS} = 7.5V$.

Then:

$$W_{REG(MAX)} \approx 400mW(MAX)$$

The maximum RMS current in M1 is calculated from the equation (30) as $I_{D(M1)} = 0.73A$. The peak current in M1 is $I_{L1(PK)}+I_{L2(PK)} \approx 3A$. (Note that the maximum power dissipation in HV9931LG (SO-8) must be derated 6.3mW/°C above 25°C. Thus, the maximum operating ambient temperature needs to be less than 60°C. Using HV9931P (DIP-8) will be limited to $T_A$ < 80°C.) A larger $V_Z$ can be selected to reduce power dissipation in the HV9931.

**Step 11.** In accordance with the equations (32)-(35), the average currents in D1-D4 are:

$$I_{D1} = 0.33A,\ I_{D2} = 0.31A,\ I_{D3} = 0.64A,\ I_{D4} = 0.6A.$$

Peak currents in D1 and D4 equal to the peak current in L1 or:

$$I_{D1(PK)} = I_{D4(PK)} = I_{L1(PK)} = 2.1A.$$

The equations (36)-(38) give the reverse voltage across D1-D3, resulting in:

$$V_{R(D1)} = 562V,\ V_{R(D2)} = 368V,\ V_{R(D3)} = 188V.$$

Adding an RC snubber is recommended across D4. Reverse voltage across D4 depends on the capacitance value of $C_D$selected for this RC snubber. The snubber capacitor $CD_d$ needs to be greater than $C_{OSS}$+ $C_{j1}$, where $C_{OSS}$ is drain-to-source capacitance of M1, and $C_{j1}$ is the reverse biased junction capacitance of D1. Usually, $C_{j1}$ can be disregarded compared to the $C_{OSS}$. The typical data by Infineon shows $C_{OSS}$ < 20pF at $V_{DS}$ > 100V for SPP03N60C3. BYD57K by Philips (800V,1A, $t_{rr}$ = 75ns) can be selected for D1. The BYD57K data by Philips shows $C_j$ < 2pF at $V_R$ > 100V. By choosing $C_d$ = 200pF and $R_d$ = 2.7KΩ, we can use a 400V rectifier for D4, for example, BYD57G (400V, 1A, $t_{rr}$ = 30ns) by Philips.

Fast switching rectifiers are needed for D2 and D3. We can select D2 STTA106A (600V, 1.0A, $t_{rr}$ = 20ns) and D3 STTH102A (200V, 1.0A, $t_{rr}$ = 30ns) by STMicroelectronics.

**Step 12.** Output filter capacitor $C_O$ of a few hundred nanofarads will be needed for improved EMI performance. Alternatively, a larger value of this capacitor can be used to reduce the switching ripple current in the LEDs further.



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