Designing a Boost-Buck (Ĉuk) Converter with the HV9930 / AT9933

A boost-buck (also known as a Ĉuk) converter is a single-switch converter, which consists of a cascade of a boost converter followed by a buck converter. A typical boost-buck converter (used as an LED driver) is shown in Figure 1.

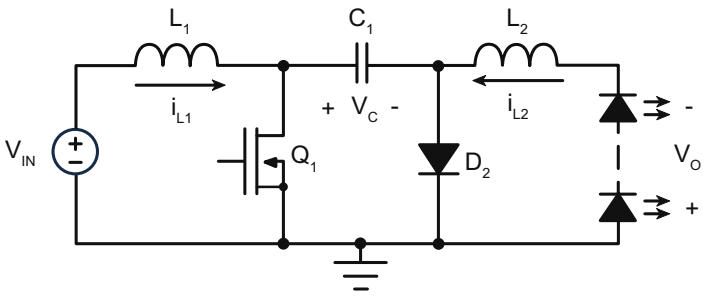

Figure 1. Boost Buck (Ĉuk) Converter

The converter has many advantages:

1. ***Automatic boost and buck operation.*** The converter can both boost and buck the input voltage. Thus, it is ideal for cases where the output LED string voltage can be either above or below the input voltage based on the operating condition.
2. ***Continuous input and output currents.*** The converter has inductors on both the input and output sides. Operating both stages in continuous conduction mode (CCM) will enable continuous currents in both inductors with low current ripple, which would greatly reduce the filter capacitor requirements at both input and output. Continuous input current would also help greatly in meeting conducted EMI standards at the input.
3. ***Localized switching.*** All the switching nodes in the circuit are isolated between the two inductors. The input and output nodes are relatively quiet. This will minimize the radiated EMI from the converter and with proper layout and design the converter can easily meet radiated EMI standards.
4. ***Failure of the switching FET.*** One of the advantages of the boost-buck converter is the capacitive isolation. The failure of the switching transistor will short the input and not affect the output. Thus, the LEDs are protected from failure of the FET.

In spite of the myriad advantages of the converter, a couple of significant disadvantages exist which prevent this converter from being used frequently.

1. ***The converter is difficult to stabilize.*** Complex compensation circuitry is often needed to make the converter operate properly. This compensation also tends to slow down the response of the converter, which inhibits the PWM dimming capability of the converter (essential for LEDs).
2. ***An output current controlled boost-buck converter tends to have an uncontrolled and undamped L–C pair (L_1 and C_1).*** The resonance of L_1 and C_1 leads to excessive voltages across the capacitor, which can damage the circuit.

The damping of L_1 and C_1 can easily be achieved by adding a damping R-C circuit across C_1. However, the problem of compensating the circuit so that it is stable is more complex.

The HV9930 solves the problem of compensation and achieving a fast PWM dimming response by using hysteretic current mode control. This ensures fast response and accurate current levels. However, a simple hysteretic current mode control would not work, as the converter would not be able to start-up. The HV9930 solves this problem by having two hysteretic current mode controllers – one for the input current and another for the output current.

During start-up, the input hysteretic controller dominates and the converter is in input current limit mode. Once the output current has built up the required value, the output hysteretic controller takes over. This approach will also help in limiting the input current in the case of an output overload or input under voltage conditions. Three resistors (for each hysteretic controller) help to set both the current ripple and the average current simplifying the controller design.

This application note will detail the operation of the boost-buck converter and the design of a HV9930 based converter. This application note can also be used to design with the AT9933. The design example is specifically designed for automotive applications, but it can also be applied for any DC/DC applications.

Operation of a Boost-Buck Converter

The diagram of a boost-buck converter is shown in Figure 1.

In steady state, the average voltages across both L_1 and L_2 are 0. Thus, the voltage across the middle capacitor is equal to the sum of the input and output voltages.

$$V_C = V_{IN} + V_O \quad (1)$$

When switch Q_1 is turned on (Figure 2a), the currents in both inductors start ramping up.

$$L_1 \frac{di_{L1}}{dt} = V_{IN} \quad (2a)$$

$$L_2 \frac{di_{L2}}{dt} = V_C - V_O = V_{IN} \quad (2b)$$

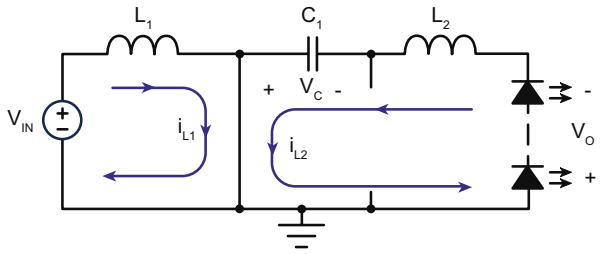

Figure 2a. Switch is turned ON

When switch Q1 is turned off (Figure 2b), the currents in both inductors start ramping down.

$$L_1 \frac{di_{L1}}{dt} = V_{IN} - V_C = -V_O \quad (3a)$$

$$L_2 \frac{di_{L2}}{dt} = -V_O \quad (3b)$$

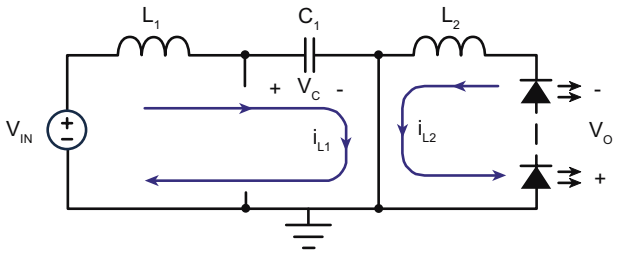

Figure 2b. Switch is turned OFF

Assuming that the switch is ON for a duty cycle D and using the fact that in steady state the total volt-sec applied across any inductor is zero, we get:

$$V_{IN} \bullet D = V_O \bullet (1\text{-}D) \Rightarrow \frac{V_O}{V_{IN}} = \frac{D}{1 - D} \quad (4)$$

Thus, the voltage transfer function obtained for the boost-buck converter will give bucking operation for D<0.5 and boosting operating for D>0.5. The steady state waveforms for the converter are shown in Figure 3.

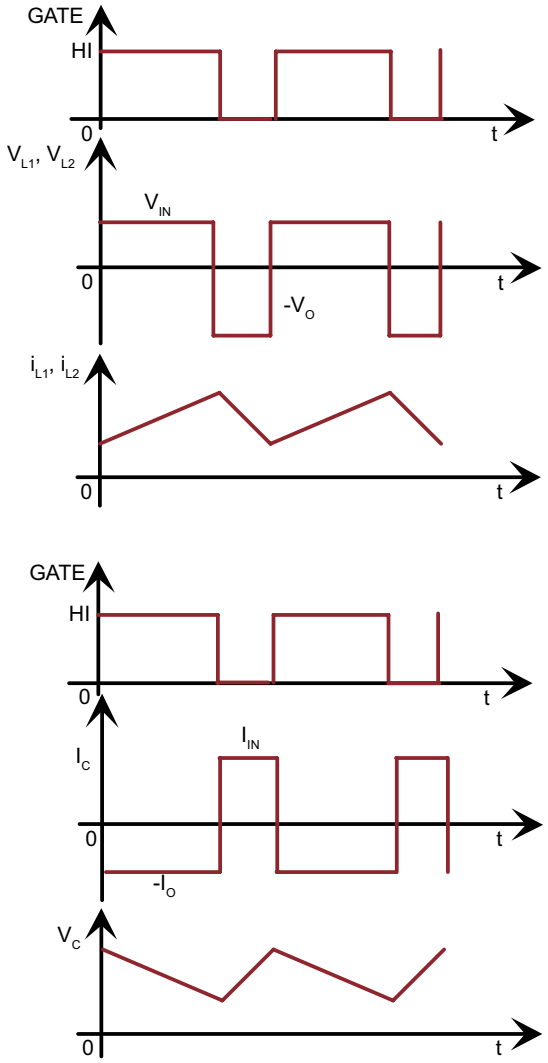

Figure 3. Steady State Waveforms

The maximum voltage seen by Q_1 and D_1 is equal to the voltage across the capacitor C_1.

$$V_{Q1} = V_{D1} = V_C \quad (5)$$

The standard boost-buck converter is modified by adding a couple of additional components for proper operation with the HV9930 (Figure 4).

1. A damping circuit R_D-C_D has been added to damp the L_1-C_1 pair.
2. An input diode (D_2) has been added. This diode is necessary for PWM dimming operation (in case of automotive applications, this could be the reverse polarity protection diode). This diode helps to prevent capacitors C_1 and C_D from discharging when the gate signals for Q_1 are turned off. Thus, when the HV9930 is enabled, the circuit is already in steady state and will reach the steady-state output current level quickly.

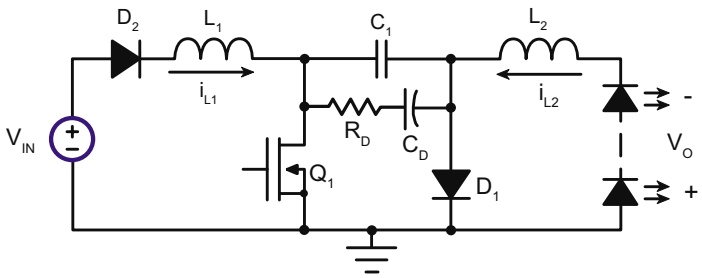

Figure 4. Modified Boost-Buck Converter

Hysteretic Control of the Boost-Buck Converter

Hysteretic control refers to the control scheme where the controlled variable (in this case, the inductor current i_{L2}) is maintained between pre-set upper and lower boundaries. As can be seen from Figure 3, the inductor current ramps up when the switch is ON and ramps down when the switch is OFF. Thus, the hysteretic control scheme turns the switch OFF when the inductor current reaches the upper limit and turns the switch ON when it reaches the lower limit. The average inductor current is then set at the average of the upper and lower thresholds. The ON and OFF times (and thus the switching frequency) vary as the input and output voltages change to maintain the inductor current levels. However, in any practical implementation of hysteretic control, there will be comparator delays involved. Thus, the switch will not turn ON and OFF at the instant the inductor current hits the limits, but after a finite (and non-zero) delay time, as illustrated in Figure 5.

This delay time introduces a couple of unwanted effects:

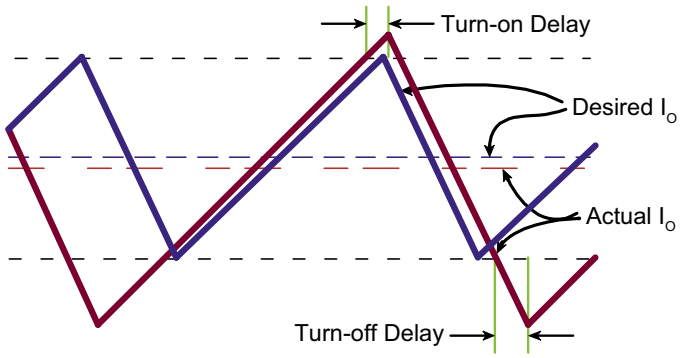

Figure 5. Hysteretic Control - Ideal & Actual

1. It alters the average value. If the down slope of the inductor current is more than the up slope, then the average value decreases and vice versa.
2. It decreases the switching frequency, which might make it tougher to meet EMI regulations.

Thus, these effects will have to be taken into consideration when designing the output inductor and the setting the current limits.

Assume a peak-to-peak current ripple setting of Δi_O (using the programming resistors) and a desired average current I_O. A hysteretic current controlled boost-buck converter acts as a constant-off-time converter as long as the output voltage is fixed, and the off-time is theoretically independent of the input voltage. Thus, the converter is designed assuming a constant off time T_{OFF} (the method to determine the off-time will be discussed later in the application note).

For the HV9930, as long as the switching frequencies are less than 150kHz, these delay times have a negligible effect and can be ignored. In these cases, the output inductor can be determined by:

$$L_2 = \frac{V_O \bullet T_{OFF}}{\Delta i_O} \qquad (6)$$

If the inductor chosen is significantly different from the computed value, the actual off-time $T_{OFF,AC}$ can be re-computed using the same equation.

However, in automotive applications, it is advantageous to set the switching frequency of the converter below 150kHz or in the range between 300kHz and 530Khz. This will place the fundamental frequency of the conducted and radiated

EMI outside of the restricted bands making it easier for the converter to pass automotive EMI regulations. In cases where the switching frequency is more than 300kHz, the delay times cannot be neglected and have to be accounted for in the computations.

Figure 6 illustrates the output inductor current waveform and the various rise and fall times. From this figure:

$$T_{OFF} = T_{f1} + T_{f2} + T_f = \frac{V_{IN}}{V_O} \bullet T_r + T_{f2} + T_f \quad (7)$$

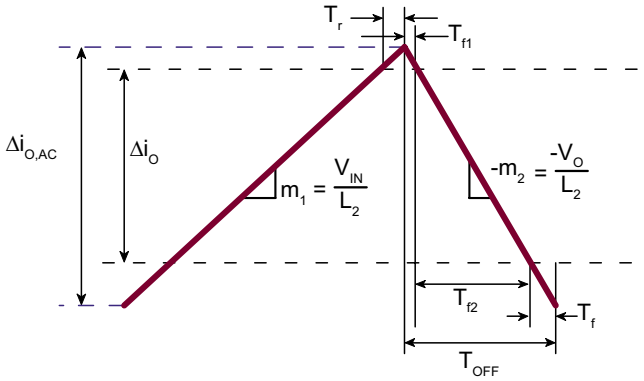

Figure 6. Hysteretic Control with Comparator Delays

T_{f2} depends on the desired output current ripple Δi_O and the down-slope of the inductor current m_2. T_r and T_f depend on the delay times of the HV9930. For the HV9930, the delay time of the comparators is related to the overdrive voltage (voltage difference between the two input terminals of the current sense comparator) applied as:

$$T_{DELAY} \approx \frac{K}{\sqrt[3]{m \bullet \frac{0.1}{\Delta i_O}}} \quad (8)$$

where m is the rising or falling slope of the inductor current.

Using (6) and the parameters of the HV9930, the equations for the parameters in (7) become,

$$T_r = \frac{6\mu}{\sqrt[3]{\frac{V_{IN} \bullet 0.1}{\Delta i_O}}} \bullet \sqrt[3]{L_2} = K_1 \bullet \sqrt[3]{L_2} \quad (9)$$

$$T_{f2} = \frac{\Delta i_O \bullet L_2}{V_O} = K_2 \bullet L_2 \quad (10)$$

$$T_f = \frac{6\mu}{\sqrt[3]{\frac{V_O \bullet 0.1}{\Delta i_O}}} \bullet \sqrt[3]{L_2} = K_3 \bullet \sqrt[3]{L_2} \quad (11)$$

Substituting (9), (10) and (11) in (7) results in a cubic equation for $\sqrt[3]{L_2}$. This cubic has one real root and two complex roots. The inductor value is the real root of the cubic raised to the third power.

$$a = K_2 \quad (12)$$

$$b = \frac{V_{IN}}{V_O} \bullet K_1 + K3$$

$$c = T_{OFF}$$

$$\Delta = 12 \bullet \sqrt{3} \bullet \sqrt{\frac{4 \bullet b^3 + 27 \bullet a \bullet c^2}{a}} \quad (13)$$

$$L_2 = \left\{ \frac{1}{6 \bullet a} \left[(108 \bullet c + \Delta) \bullet a^2 \right]^{1/3} - \frac{2 \bullet b}{\left[(108 \bullet c + \Delta) \bullet a^2 \right]^{1/3}} \right\}^3 \quad (14)$$

The actual off-time $T_{OFF,AC}$ can be computed by substituting the chosen inductor value back into (7). The actual ripple in the inductor current $\Delta i_{O,AC}$ is:

$$\Delta i_{O,AC} = \frac{V_O \bullet T_{OFF,AC}}{L_2} \quad (15)$$

R-C Damping of the Boost-Buck Converter

The single-switch boost-buck converter has been derived by cascading boost and buck converters, (in that order), and driving both switches with the same signal (Figure 7). The relationships between the voltages in the system are:

$$\frac{V_C}{V_{IN}} = \frac{1}{1 - D} \quad \textit{(boost converter)} \quad (16)$$

$$\frac{V_O}{V_C} = D \quad \textit{(buck converter)}$$

The capacitor voltage V_C and the input-output relationship can both be derived using (16).

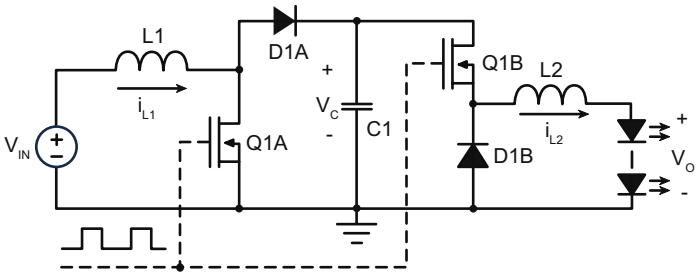

Figure 7. Boost-Buck Converter

$$\frac{V_O}{V_{IN}} = \frac{V_O}{V_C} \bullet \frac{V_C}{V_{IN}} = \frac{D}{1\text{-}D} \tag{17}$$

$$V_C = \frac{V_{IN}}{1\text{-}D} = \frac{V_{IN}}{1 - (V_O / V_C)} \tag{18}$$

$$\Rightarrow V_C = V_O + V_{IN}$$

For the purposes of designing the damping network, it is easier to visualize the converter in its two-switch format of Figure 7 rather than as the single switch Ĉuk converter. Hence, for the remainder of this section, the cascaded converter will be used to derive the equations.

In hysteretic control of the boost-buck converter using the HV9930, the output buck stage is controlled and the input boost stage is uncontrolled. An equivalent schematic of the HV9930 controlled boost-buck converter is shown in Fig. 8.

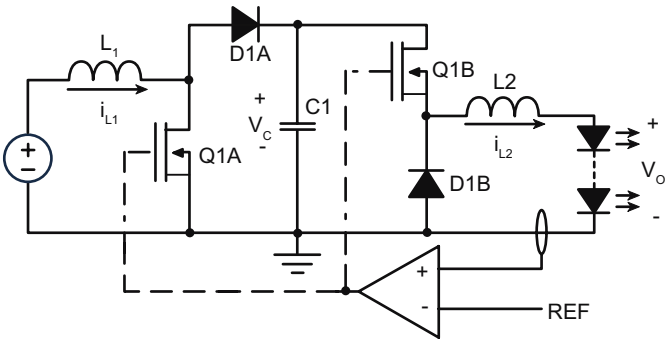

Figure 8. Hysteretic Control of the Buck Stage

The hysteretic control of the buck stage ensures that the output current i_{L2} is constant under all transient conditions. So, for the purposes of average modeling, the load seen by the capacitor C_1 can be modeled as a current source equal to $d \bullet I_O$, where d is the instantaneous duty cycle and I_O is the constant output current. The continuous conduction mode buck stage also imposes one more constraint:

$$V_O = d \bullet V_C \tag{19}$$

where d and V_C are the time dependent duty cycle and capacitor voltage and V_O is the constant output voltage. These constraints can be modeled as shown in Figure 9. The figure shows that the current loop for the output current control also imposes another loop for the control of the capacitor voltage. For the system to be stable, it is necessary that this capacitor voltage loop also be stable.

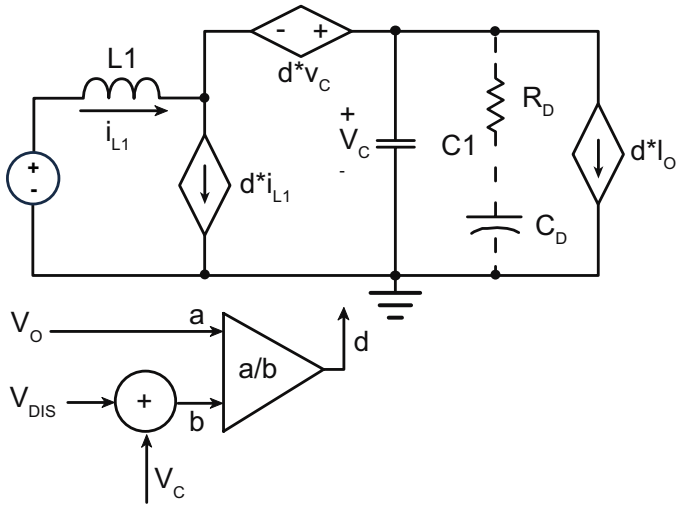

Figure 9. Average Model of Controlled Boost-Buck Converter

Figure 9 also includes an external source V_{DIS}. This is a disturbance input (simulates a perturbation in the capacitor voltage). Typically, for a stable system, the effect of the disturbance on the system should be rejected.

The loop gain of the system for a boost-buck converter without damping is shown in Figure 10 (Green - Magnitude and Red - Phase).

It can be seen that the phase margin of the system is negative (i.e. the phase is less than -180^O when the magnitude crosses 0dB). This is due to the undamped LC pole-pair and causes the system to be unstable. Thus, any disturbance to the capacitor voltage will get amplified an keep increasing till the components breakdown.

R – C damping of this undamped pole pair can stabilize the system and make sure that the disturbance input is properly damped. Also, the presence of C_D ensures that R_D will not see the DC component of the voltage V_C across it, reducing

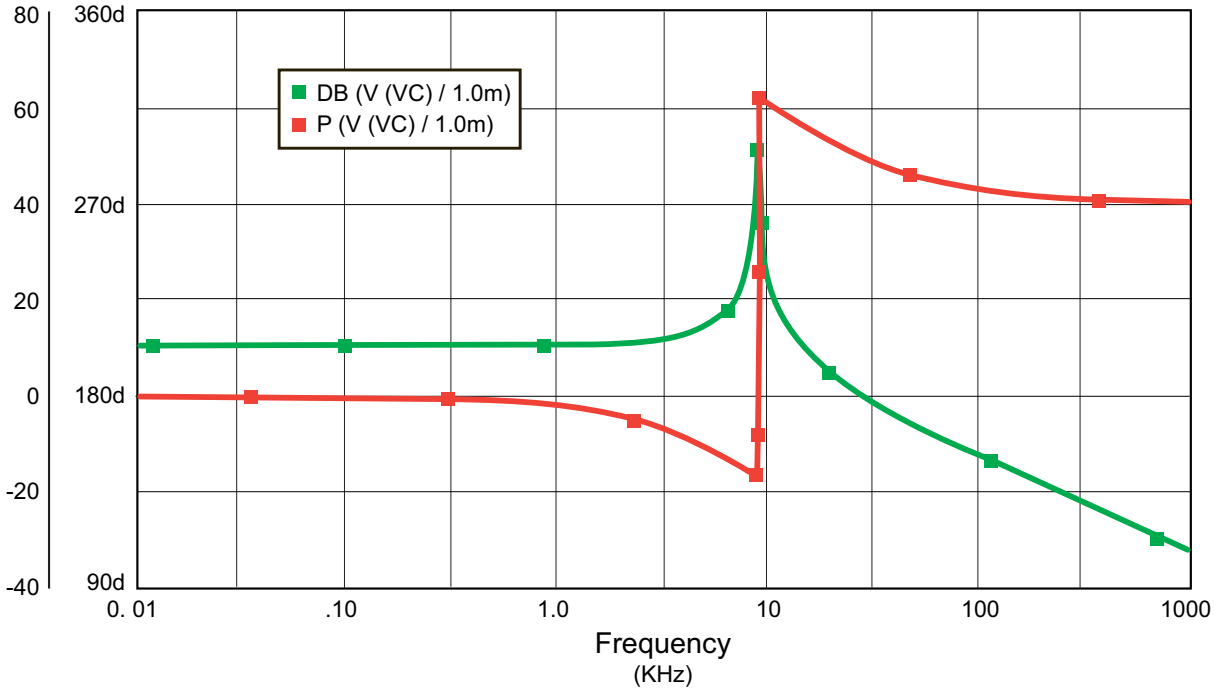

Figure 10. UndampedBoost-Buck Converter

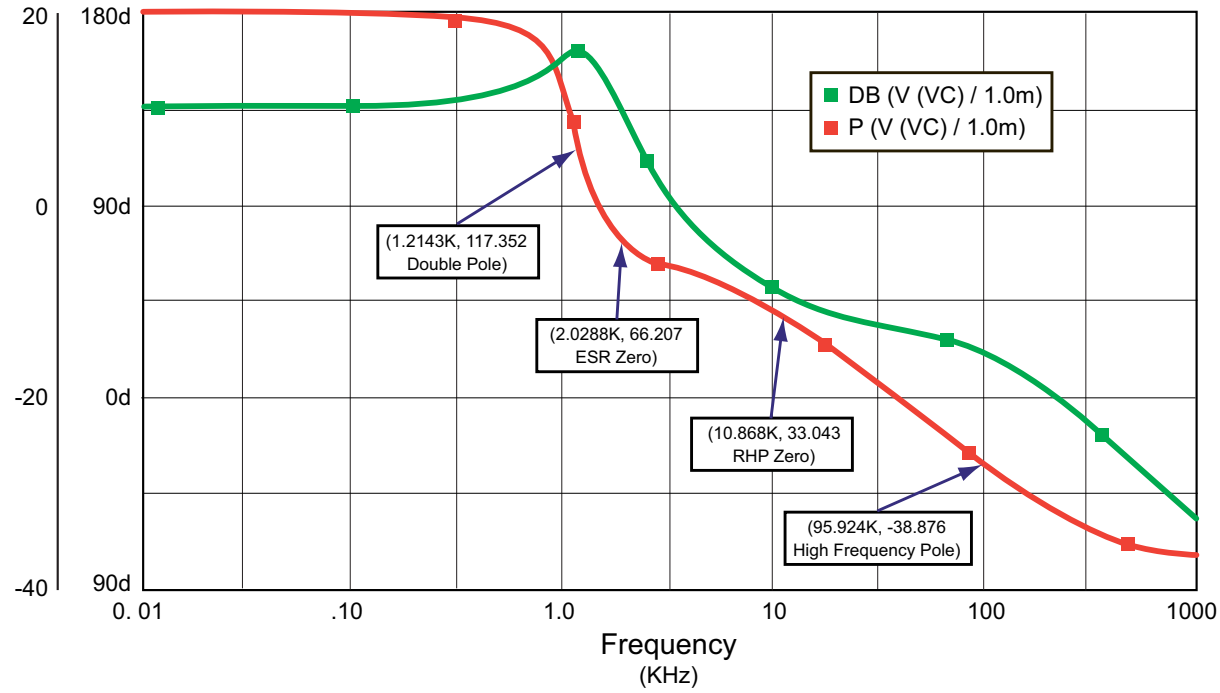

Figure 10. DampedBoost-Buck Converter

the power dissipated in the damping resistor (C_D blocks the DC component of the voltage).

Figure 11 shows the Bode plot of the loop gain for the same system with an appropriate damping network (Green – Magnitude and Red – Phase). It can be seen that the system is now stable.

Using the model of Figure 9 and assuming $C_D >> C_1$, the loop gain transfer function of the R – C damped boost-buck converter can be derived as:

$$G(s)H(s) = \frac{D}{1-D} \bullet \frac{(1 + s \bullet R_D \bullet C_D) \bullet \left(1 - s \bullet \frac{D}{(1 - D)^2} \bullet \frac{L_1 \bullet I_O}{V_O}\right)}{(1 + s \bullet R_D \bullet C_1) \bullet \left(1 + s \bullet R_D \bullet C_D + s^2 \bullet \frac{L_1 \bullet C_D}{(1 - D)^2}\right)} \quad (20)$$

Thus, the loop has a DC gain of D/(1-D) and includes:

1) *Damping (and ESR) zero at* $\omega_Z = (R_D \bullet C_D)^{-1}$;
2) *RHP zero at* $\omega_{RHP} = \frac{(1 - D)^2}{D} \bullet \frac{V_O}{L_1 \bullet I_O}$;
3) *Complex double pole with natural resonant frequency* $\omega_O = \frac{1 - D}{\sqrt{L_1 \bullet C_D}}$ *and quality factor* $Q = (1 - D) \bullet R_D \bullet \sqrt{\frac{C_D}{L_1}}$
4) *High-frequency pole at* $\omega_P = (R_D \bullet C_1)^{-1}$.

In order to achieve stable loop, the 0dB crossing (ω_C) must be placed such that $\omega_C << \omega_{RHP}$ and $\omega_C << \omega_P$. The latter condition is easily met by selecting $C_D >> C_1$.

We can easily obtain approximate values of C_D and R_D for the case of $\omega_C >> \omega_O$. This condition is usually met for the worst-case calculations at minimum input voltage, since the DC gain is the highest at this condition. Set $\omega_C = \omega_{RHP} / N$, where N >> 1. Then ω_O can be approximately calculated from:

$$\omega_O = \omega_C \bullet \sqrt{\frac{1 - D}{D}} = \frac{\omega_{RHP}}{N} \bullet \sqrt{\frac{1 - D}{D}} \quad (21)$$

Substituting for ω_O and ω_{RHP} in (21) gives the equation for computing C_D:

$$C_D = \frac{N^2 \bullet D^3}{(1 - D)^3} \frac{L_1 \bullet I_O^2}{V_O^2} \quad (22)$$

Selecting R_D such that $\omega_Z = \omega_C$ results in a good phase margin with minimum power dissipation. Then, using equations for ω_Z and ω_{RHP} gives a solution for R_D.

$$R_D = \frac{N \bullet D}{(1 - D)^2} \frac{L_1 \bullet I_O}{C_D \bullet V_O} \quad (23)$$

The approximate values for the damping network can be computed using the following equations (derived from (22) and (23) assuming N = 3).

$$C_D = 9 \bullet [D / (1 - D)]^3 \bullet L_1 \bullet (I_O / V_O)^2 \quad (24)$$

$$R_D = \frac{3 \bullet D}{(1 - D)^2} \bullet \frac{L_1 \bullet I_O}{C_D \bullet V_O} \quad (25)$$

Note that the damping resistor value includes the ESR of the damping capacitor. In many cases, the damping capacitor is chosen to be an electrolytic capacitor, which will have a significant ESR. In such cases, the damping resistor can be reduced accordingly.

Dimming Ratio Using PWM Dimming

The linearity in the dimming ratio achievable with the HV9930 depends on both the switching frequency and the PWM dimming frequency.

For a converter designed to operate at a minimum switching frequency of 300kHz, one switching time period equals 3.33µs. This is the minimum on-time of the PWM dimming cycle. At a PWM dimming frequency of 200Hz (5ms period), 3.33µs equals a minimum duty cycle of 0.067%. This corresponds to a 1:1500 dimming range. However, the same converter being PWM dimmed at 1.0kHz (1ms time period) will have a minimum duty ratio of 0.33% or a PWM dimming range of 1:300.

If the minimum on-time of the PWM dimming cycle is less than the switching time period, the LED current will not reach its final value. Hence the average current will be less. Thus, the LEDs will dim, but there will be a loss of linearity between the average LED current and the duty cycle of the PWM input.

Design of the Boost-Buck converter with HV9930

Consider a boost-buck converter with the following parameters (Figure 1-1).

Input Voltage:

$V_{IN,MIN}$ = *9.0V*

$V_{IN,NOM}$ = *13.5V*

$V_{IN,MAX}$ = *16V*

$V_{IN,TR}$ = *42V* *(Clamped load dump rating)*

$V_{IN,REV}$ = *-14V* *(Reverse polarity voltage)*

Load:

V_O = *28V*

I_O = *350mA*

R_{LED} = *5.6Ω*

Estimated Efficiencies:

η_{MIN} = *0.72 (at $V_{IN,MIN}$)*

η_{NOM} = *0.80*

η_{MAX} = *0.82*

These efficiency values do not take into account the power loss in the reverse blocking diode. The diode will dissipate power in the range of *0.4 - 0.6W* and will drop about V_D = *0.5V* across it. This diode drop will be taken in account while designing the converter.

The efficiency values used in this design are typical values for the given input voltages and output power level. Higher efficiencies can be obtained at lower input current levels. The efficiency values will depend on the operating conditions. Except in very high power designs, these values can be used as a good approximation. The efficiency drop at lower input voltages is due to the larger input currents and its associated conduction losses.

Note:

Efficiencies higher than 85% can easily be achieved with the HV9930 controlled Ĉuk converter if the operating frequency is kept below 150kHz. However, for purposes of EMI compliance, the higher efficiencies are traded-off for higher switching frequencies (which increase switching losses in the system).

Design of the Power Stage

Step 1: *Choose a switching frequency at the minimum input voltage*

Although the HV9930 is a variable frequency IC, the selection of the switching frequency is an important criterion, as this will decide the point around which the actual frequency will vary. In the case of automotive converters, designing with a switching frequency in the range between 300kHz and 530kHz would avoid the restricted radio broadcast bands and make it easier to meet the conducted and radiated EMI specifications. So, choose a minimum switching frequency (which occurs at minimum input voltage) $f_{S,MIN}$ = *300kHz*.

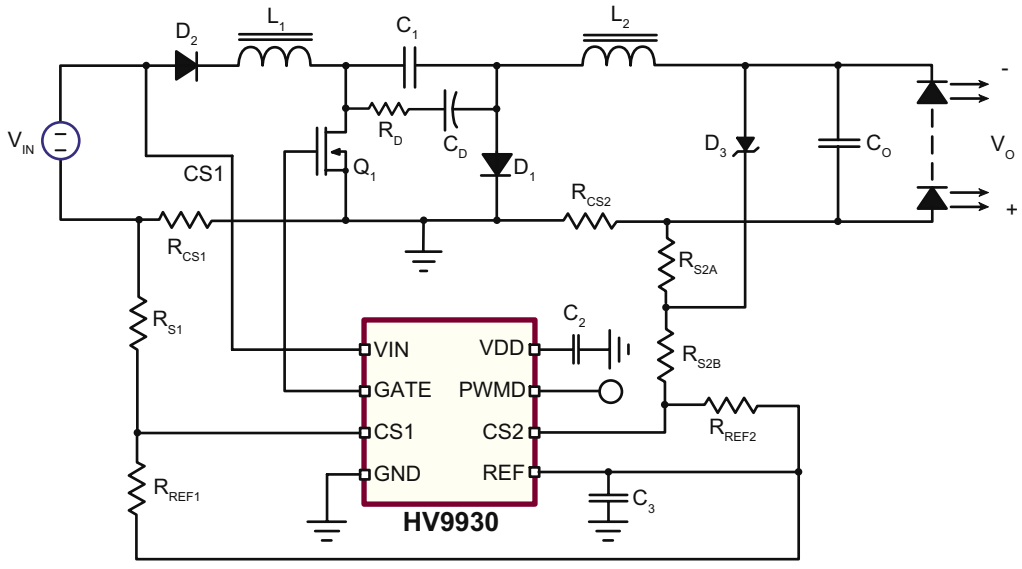

Figure 1-1. DampedBoost-Buck Converter

Step 2: *Compute the duty cycle*

The duty cycle of operation will have to be computed at the minimum input voltage:

$$D_{MAX} = \frac{1}{1 + \frac{\eta_{MIN} \bullet (V_{IN,MIN} - V_D)}{V_O}} \quad (1\text{-}1)$$

$$= 0.821$$

Step 3: *Compute the input current values*

The input current level at the minimum input voltage needs to be computed. The value obtained will be used to compute the current ratings of the various components:

$$I_{IN,MAX} = \frac{V_O \bullet I_O}{\eta_{MIN} \bullet (V_{IN,MIN} - V_D)} \quad (1\text{-}2)$$

$$= 1.601A$$

Step 4: *Compute the output inductor*

The first step is to compute the off-time. The off-time of the converter can be calculated as:

$$T_{OFF} = \frac{1 - D_{MAX}}{f_{S,MIN}} \quad (1\text{-}3)$$

$$= 598ns$$

Assuming a 25% peak-to-peak ripple in the output current ($\Delta i_O = 87.5mA$), and accounting for the diode drop in the input voltage by substituting $V_{IN,MIN} - V_D$ in place of V_{IN}, equation (7) yields:

$$598ns = 0.887\mu \bullet \sqrt[3]{L_2} + 3.125m \bullet L_2 + 1.89\mu \bullet \sqrt[3]{L_2} \quad (1\text{-}4)$$

Solving for L_2 using (12), (13) and (14) gives:

$$L_2 = (0.052)^3 = 145\mu H$$

The closest standard value inductor is a 150µH, 0.35A rms, 0.4A sat inductor.

Since the inductance value is different from the computed value, the actual off-time will also change as:

$$T_{OFF,AC} = 2.777\mu \bullet \sqrt[3]{L_{2,AC}} + 3.125m \bullet L_{2,AC} \quad (1\text{-}5)$$

$$= 616ns$$

The actual ripple in the output current is given by:

$$\Delta i_{O,AC} = \frac{V_O \bullet T_{OFF,AC}}{L_{2,AC}} \quad (1\text{-}6)$$

$$= 0.115A$$

Note that although the ripple in the output current was assumed to be about 25% (or 87.5mA), the actual ripple is almost double that value. This increase in the ripple is due to the delays of the comparators. A capacitor will be required at the output of the converter (across the LEDs) to reduce the ripple to the desired level. This capacitor will be very small as the switching frequencies are large.

It is also useful to compute the ripple overshoot and undershoot beyond the programmed limits. This will help determine how the average current changes due to the delays.

$$\Delta i_{OVER} = \frac{V_O}{L_{2,AC}} \bullet \left(\frac{V_{IN,MIN} - V_D}{V_O} \bullet K_1 \right) \bullet \sqrt[3]{L_{2,AC}} \quad (1\text{-}7)$$

$$= 8.3mA$$

$$\Delta i_{UNDER} = \frac{V_O}{L_{2,AC}} \bullet K_3 \bullet \sqrt[3]{L_{2,AC}} \quad (1\text{-}8)$$

$$= 19mA$$

Thus, the average output current will be reduced from the set value by about 10.7mA.

In most cases, due to the inductor values available, the actual off-time will differ from the computed value significantly. Thus, it is better to use the actual value of the off-time computed in (1-5) hereon to compute the rest of the values.

Note:

If the switching frequency is less than 150kHz, equation (6) can be used to compute the output inductance value, simplifying the procedure greatly.

Step 5: *Compute the input inductor*

Assuming a 15% peak-to-peak ripple (this low input ripple will minimize the input filtering capacitance needed) in the input current at minimum input voltage and the off-time computed in (1-5), the input inductor can be computed as:

$$L_1 = \frac{V_O \bullet T_{OFF,AC}}{0.15 \bullet I_{IN,MAX}} \quad (1\text{-}9)$$

$$= 72\mu H$$

The closest standard value inductor is an 82µH inductor. The current rating of this inductor will be decided in the final stages after the input current limit has been set.

The peak-to-peak ripple in the input current is:

$$\Delta i_{OVER} = \frac{V_O \bullet T_{OFF,AC}}{L_{1,AC}} \quad (1\text{-}10)$$

$$= 0.21A$$

Step 6: *Compute the value of the middle capacitor*

Assuming a 10% ripple across the capacitor at minimum input voltage ($\Delta V_C = 0.1 \bullet (V_{IN,MIN} - V_D + V_O) = 3.65V$), capacitor C_1 can be computed as:

$$C_1 = \frac{I_{IN,MAX} \bullet T_{OFF,AC}}{\Delta V_C} \quad (1\text{-}11)$$

$$= 0.257\mu F$$

$$I_{RMS,C1} = \sqrt{I_{IN,MAX}^2 \bullet (1 - D_{MAX}) + I_O^2 \bullet D_{MAX}} \quad (1\text{-}12)$$

$$= 0.72A$$

The voltage rating and type of this capacitor have to be chosen carefully. This capacitor carries both the input current and the output current. Thus, to prevent excessive losses and overheating of the capacitor, it must have a very low ESR. Ceramic capacitors are an ideal choice for this application due to their low ESR and high transient voltage limit. The maximum steady state voltage across the capacitor is 44V (28V + 16V), and the maximum transient voltage across the capacitor $V_{C,MAX}$ is 70V (28V + 42V). Ceramic capacitors can easily withstand up to 2.5 times their voltage rating for the duration of the load dump voltage. Also, the actual capacitance value of these capacitors reduces based on the bias voltage applied. Ceramic capacitor types X7R and X5R are more stable and the capacitance drop is not more than 20% at full rated voltage.

Thus, a 0.22µF, 50V X7R ceramic chip capacitor can be chosen.

Step 7: *Choose the Switching Transistor*

The peak voltage across the MOSFET Q_1 is 70V. Assuming a 30% overhead on the voltage rating to account for leakage inductance spikes, the MOSFET voltage needs to be at least:

$$V_{FET} = 1.3 \bullet V_{C,MAX} \quad (1\text{-}13)$$

$$= 91V$$

The rms current through the FET will be maximum at low input voltage (higher current levels and maximum duty cycle). The maximum rms current through the FET is:

$$I_{FET,MAX} = (I_{IN} + I_O) \bullet \sqrt{D_{MAX}} \quad (1\text{-}14)$$

$$= 1.77A$$

A typical choice for the MOSFET is to pick one whose current rating is about three times the maximum rms current. Choose a FDS3692 from Fairchild Semiconductors (100V, 4.5A, 50mΩ N-channel MOSFET).

Note:

The C_{ISS} of the chosen FET is about 750pF. It is recommended that the FET input capacitance not exceed 1000pF, as the large switching times will cause increased switching losses. A FET with an input capacitance around 500pF would be ideal. A higher input capacitance would be allowable if the switching frequency can be reduced appropriately.

Step 8: *Choose the switching diode*

The maximum voltage rating of the diode D_2 is the same as the FET voltage rating. The average current through the diode equal to the output current.

$$I_{DIODE} = I_O = 350mA \quad (1\text{-}15)$$

Although the average current of the diode is only 350mA, the actual switching current through the diode goes as high as 1.95A ($I_{IN,MAX} + I_O$). A 500mA diode will be able to carry the 1.79A current safely, but the voltage drop at such high current levels would be extremely large increasing the power dissipation. Thus, we need to choose a diode whose current rating is at least 1.0A.

Choose B2100-13 by Diodes, Inc. (100V, 2A Schottky diode).

Step 9: *Choose the Input Diode*

The input diode serves two purposes:

1. It protects the circuit from a reverse polarity connection at the input.
2. It helps in PWM dimming of the circuit by preventing C_1 from discharging when the HV9930 is turned off.

The current rating of the device should be at least equal to $I_{IN,MAX}$. The voltage rating of the device should be more than the reverse input voltage rating.

Choose B220-13 by Diodes, Inc. (20V, 2A schottky diode).

Step 10: *Designing the input capacitance*

Some capacitance is required on the input side to filter the input current. This capacitance is mainly responsible for reducing the 2ND harmonic of the input current ripple (which in this case falls in the AM band). According to the SAE J1113 specifications, the peak limit for narrowband emissions in this range is 50dBµV to meet Class 3 at an input voltage of 13 +/- 0.5V. Assuming a saw tooth waveform for the input current as a conservative approximation, the rms value of the 2ND harmonic component of the input current ($I_{IN,2}$) can be computed as:

$$I_{IN,2} = \frac{\Delta I_{IN}}{2\sqrt{2} \bullet \pi} = 0.024A \quad (1\text{-}16)$$

The switching frequency of the converter at 13V input can be computed as:

$$D_{NOM} = \frac{1}{1 + \frac{\eta_{NOM} \bullet (V_{IN,NOM} - V_D)}{V_O}} \quad (1\text{-}17)$$

$$= \frac{1}{1 + \frac{0.8 \bullet (13.5 - 0.5)}{28}}$$

$$= 0.73$$

$$f_{S,NOM} = \frac{1 - D_{NOM}}{T_{OFF,AC}} \quad (1\text{-}18)$$

$$= 414kHz$$

$$C_{IN} = \frac{I_{IN,2}}{4\pi \bullet f_{S,NOM} \bullet 10^{-6} \bullet 10^{50/20}} \quad (1\text{-}19)$$

$$= 14.6\mu F$$

Choose a parallel combination of 4.7µF, 25V, X7R ceramic capacitor.

Step 11: *Designing the Output Capacitance*

The value of the output capacitance required to reduce the LED current ripple from 115mA to $\Delta I_{LED} = 70mA$ (20% peak to peak ripple) can be approximately computed by using only the first harmonic in the inductor current. A 70mA peak-to-peak ripple in the LED results in a 392mV ($\Delta v_O = \Delta I_{LED} \bullet R_{LED}$) peak to peak ripple voltage. Then:

$$\frac{\Delta v_O}{2} = \frac{8}{\pi^2} \bullet \frac{\Delta i_{L2}}{2} \bullet \frac{R_{LED}}{\sqrt{1 + (2\pi \bullet f_{S,MIN} \bullet R_{LED} \bullet C_O)^2}} \quad (1\text{-}20)$$

The output capacitance required can then be computed from (1-20) as:

$$C_O = \frac{\sqrt{\left(\frac{8 \bullet R_{LED}}{\pi^2} \bullet \frac{\Delta i_{L2}}{\Delta v_O}\right)^2 - 1}}{2\pi \bullet f_{S,MIN} \bullet R_{LED}} \quad (1\text{-}21)$$

$$= 0.083\mu F$$

Use a 0.10µF, 35V ceramic capacitor.

Step 11: *Computing the Theoretical Switching Frequency Variation*

The maximum and minimum frequencies (using steady state voltage conditions) can be computed as:

$$f_{S,MIN} = \frac{1 - \frac{1}{1 + \eta_{MIN} \bullet (V_{IN,MIN} - V_D) / V_O}}{T_{OFF,AC}} \quad (1\text{-}22)$$

$$= 291kHz$$

$$f_{S,MAX} = \frac{1 - \frac{1}{1 + \eta_{MAX} \bullet (V_{IN,MAX} - V_D) / V_O}}{T_{OFF,AC}} \quad (1\text{-}23)$$

$$= 506kHz$$

The theoretical frequency variation for this design is 398kHz ± 27%.

Design of the Damping Circuit

The values for the damping network can be computed using (20) and (21).

$$C_D = 9 \bullet \left(\frac{D_{MAX}}{1 - D_{MAX}}\right)^3 \bullet L_{1,AC} \bullet \left(\frac{I_O}{V_O}\right)^2 \quad (1\text{-}24)$$

$$= 11\mu F$$

$$R_D = \frac{3 \bullet D_{MAX}}{(1 - D_{MAX})^2} \bullet \frac{L_{1,AC} \bullet I_O}{C_D \bullet V_O} \quad (1\text{-}25)$$

$$= 7.16\Omega$$

The power dissipated in R_D can be computed as:

$$P_{RD} = \frac{\Delta v_C^2}{12 \bullet R_D} \quad (1\text{-}26)$$

$$= \frac{3.65^2}{12 \bullet 7.16} = 0.155W$$

The rms current through the damping capacitor will be:

$$i_{CD} = \frac{\Delta v_C}{2\sqrt{3} \bullet R_D} = 0.147A \quad (1\text{-}27)$$

Choose a 10µF, 50V electrolytic capacitor, which can allow at least 150mA rms current. An example would be the EEVFK1H100P from Panasonic (10µF, 50V, Size D). This capacitor has about a 1.0Ω ESR, so R_D can be reduced to about 6.2Ω.

Design using the HV9930

Step 11: *Internal Voltage Regulator of the HV9930*

The HV9930 includes a built-in 8.0 - 200V linear regulator. This regulator supplies the power to the IC. This regulator can be connected at either one of two nodes on the circuit based on the requirement:

1. In the normal case, when the input voltage is always greater than 8.0V, the VIN pin of the IC can be connected to the input voltage directly or with a series diode (Figure 1-2a) in case reverse polarity protection is required.
2. In conditions where the converter needs to operate at voltages lower than 8.0V, once the converter is running (as in the case of cold-crank operation), the VIN pin of the HV9930 can be connected as shown in Figure 1-2b. In this case, the drain of the FET is at V_{IN} + V_O, and hence even if the input voltage drops below 8.0V, the IC will still be functioning. However, in this case, more hold-up capacitance will be required at the VDD pin to supply the power to the IC when the FET is ON. Also, in this case, a small capacitor (1.0nF) between the VIN and GND pins of the HV9930 is recommended.
3. In both cases, a ceramic capacitance of 1.0µF of greater is recommended at the VDD pin.

Step 12: *Internal Voltage Reference*

The HV9930 includes an internal 1.25V (+/-3%) reference. This reference can be used to set the current thresholds for the input and output hysteretic comparators. It is recommended that this pin be bypassed with at least a 0.1µF ceramic capacitor.

Step 13: *Programming the Hysteretic Controllers and Over Voltage Protection*

The input and output current levels for the hysteretic controllers are set by means of three resistors for each current

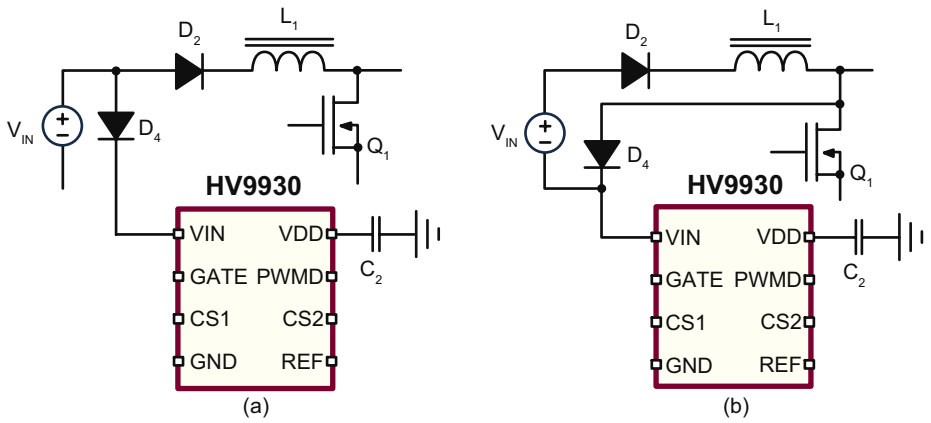

Figure 1-2. Connecting the VIN Pin of the HV9930

- one current sense resistor and two divider resistors. The equations governing the resistors are the same for both the input and output sides and are given as:

$$\frac{R_S}{R_{REF}} = \frac{0.05 \bullet (\Delta i / I) + 0.1}{1.2 \bullet (\Delta i / I) - 0.1} \quad (1\text{-}28)$$

$$R_{CS} = \frac{1.2 \bullet (R_S / R_{REF}) - 0.05}{I} \quad (1\text{-}29)$$

These equations assume that the 1.25V reference provided by the HV9930 is used to set the current. In cases where Linear Dimming of the LEDs is required, it is recommended that the input current thresholds be based on the 1.25V reference and the output current thresholds are modified using the variable input voltage available. In such a case, assuming the maximum external voltage V_{LD} as the reference, the above two equations can be modified as:

$$\frac{R_S}{R_{REF}} = \frac{0.05 \bullet (\Delta i / I) + 0.1}{(V_{LD} - 0.05) \bullet (\Delta i / I) - 0.1} \quad (1\text{-}30)$$

$$R_{CS} = \frac{(V_{LD} - 0.05) \bullet (R_S / R_{REF}) - 0.05}{I} \quad (1\text{-}31)$$

In this design example, it is assumed that Linear Dimming is not required and the 1.25V reference is used for both the input and output programming.

Note:

The HV9930 cannot operate the boost-buck converter in the discontinuous conduction mode. Thus, if the external voltage is reduced:

$$V_{LD} = 0.1 \bullet \frac{R_{REF2} + R_{S2}}{R_{S2}}$$

the LEDs will extinguish.

The programming of the output side is also linked to the over voltage protection. The boost-buck converter is not inherently programmed against open LED conditions. Thus, external protection is required. This is done by adding zener diode D_3 and splitting the resistor R_{S2} into two parts - R_{S2A} and R_{S2B}. When there is an open LED condition, the inductor current will flow through diode D_3. This will then clamp the output voltage at the diode voltage. However, since the diode cannot take the LED current, the current level has to be reduced to more manageable levels. This is done by the combination of R_{CS2} and R_{S2A}. In normal operation, the inductor current will flow only through R_{CS2}. During open LED conditions, the current will flow though both R_{CS2} and R_{S2A}. Thus, the effective current sense resistor seen by the IC is $R_{CS2} + R_{S2A}$. This, in effect, will reduce the current level and thus prevent the high LED currents from flowing into the zener diode.

Design of the output side resistors

For the output current, $I_O = 0.36A$ (to compensate for the 10mA drop due to the delay times) and $\Delta I_O = 87.5mA$. Note that we are using the values assumed and not the actual values computed in (1-6) for the ripple current. Using these values in the above equations:

$$\frac{R_{S2A} + R_{S2B}}{R_{REF2}} = 0.534 \quad (1\text{-}32)$$

$$R_{CS2} = 1.64\Omega$$

$$R_{RCS2} = 0.35^2 \bullet 1.64 = 0.2W \quad (1\text{-}33)$$

Before we complete the design of the output side, we also have to design the over voltage protection. For this application, choose a 33V Zener diode. This is the voltage at which the output will clamp in case of an open LED condition. For a 350mW diode, the maximum current rating at 33V works out to about 10mA. Using a 5.0mA current level during open LED conditions, and assuming the same R_S / R_{REF} ratio,

$$R_{S2A} + R_{CS2} = 120\Omega \quad (1\text{-}34)$$

Choose the following values for the resistors:

$R_{CS2} = 1.65\Omega$, 1/4W, 1%
$R_{REF2} = 10k\Omega$, 1/8W, 1%
$R_{S2A} = 100\Omega$, 1/8W, 1%
$R_{S2B} = 5.23k\Omega$, 1/8W, 1%

Design of the input side resistors

For the input side, we first have to determine the input current level for limiting. This current level is dictated by the fact the input comparator must not interfere with the operation of the circuit even at minimum input voltage.

The peak of the input current at minimum input voltage will be:

$$I_{IN,PK} = I_{IN,MAX} + \frac{\Delta I_{IN}}{2} \quad (1\text{-}35)$$

$$= 1.706A$$

Assuming a 30% peak-to-peak ripple when the converter is in input current limit mode, the minimum value of the input current will be:

$$I_{LIM,MIN} = 0.85 \bullet I_{IN,LIM} \quad (1\text{-}36)$$

We need to ensure that $I_{LIM,MIN} > I_{IN,PK}$ for proper operation of the circuit. Assuming a 5% safely factor, i.e.,

$$I_{LIM,MIN} = 1.05 \bullet I_{IN,PK} \quad (1\text{-}37)$$

we can compute the input current limit to be $I_{IN,LIM} = 2.1A$

Using equations (1-28) and (1-29) and a 30% peak to peak ripple, we can compute:

$$\frac{R_{S1}}{R_{REF1}} = 0.442 \quad (1\text{-}38)$$

$$R_{CS1} = 0.228\Omega$$

$$P_{RCS1} = I_{IN,LIM}^2 \bullet R_{CS1} = 1.0W \quad (1\text{-}39)$$

This power dissipation is a maximum value, which occurs only at minimum input voltage. At a nominal input voltage of 13.5V, we can compute the input current using (1-2) and using the nominal values for the efficiency and the input voltage.

$$I_{IN,NOM} = \frac{28 \bullet 0.35}{0.8 \bullet (13.5 - 0.5)} \quad (1\text{-}40)$$

$$= 0.942A$$

$$P_{RCS1} = 0.942^2 \bullet 0.228 = 0.2W \quad (1\text{-}41)$$

Thus, at nominal input voltage, the power dissipation reduces by about 5 times to a reasonable 0.2W.

Choose the following values for the resistors:

R_{CS1} = parallel combination of three 0.68Ω, 1/2W, 5% resistors
$R_{REF1} = 10k\Omega$, 1/8W, 1%
$R_{S1} = 4.42k\Omega$, 1/8W, 1%

Step 14: *Input Inductor Current Rating*

The maximum current through the input inductor is $I_{LIM,MAX} = 1.15 \bullet I_{IN,LIM} = 2.4A$. Thus, the saturation current rating of the inductor has to be at least 2.5A. If the converter is going to be in input current limit for extended periods of time, the rms current rating needs to be 2.0A, else a 1.5A rms current rating will suffice.

Meeting Conducted and Radiated EMI

Due to the nature of the boost-buck converter, it is easy to meet conducted and radiated EMI specifications. A few precautions need to be taken during design and PCB layout to be able to meet the EMI standards.

1. In some cases, when the input current ripple is too large or the switching frequency of the converter is in the EMI band, it might not be possible to meet the conducted EMI standards using only capacitors at the input. In such cases, an input PI filter might be required to filter the low frequency harmonics.
2. Shielded inductors or toroidal inductors should always be preferred over unshielded inductors. These inductors will minimize radiated magnetic fields.
3. During layout, the ground connection (purple node in Figure 1-3) should be connected to a copper plane on one of the PCB layers with the copper plane extending under the inductors.
4. The loop consisting of Q_1, C_1 and D_1 should be as small as possible. This would help greatly in the meeting the high frequency EMI specifications.
5. The length of the trace from GATE output of the HV9930 to the GATE of the FET should be as small as possible with the source of the FET and the GND of the HV9930 being connected to the GND plane.
6. An R-C damping network might be necessary across diode D_1 to reduce ringing due to the undamped junction capacitance of the diode.

A sample layout for an EMI compliant converter can be found in the HV9930DB1 demoboard datasheet.

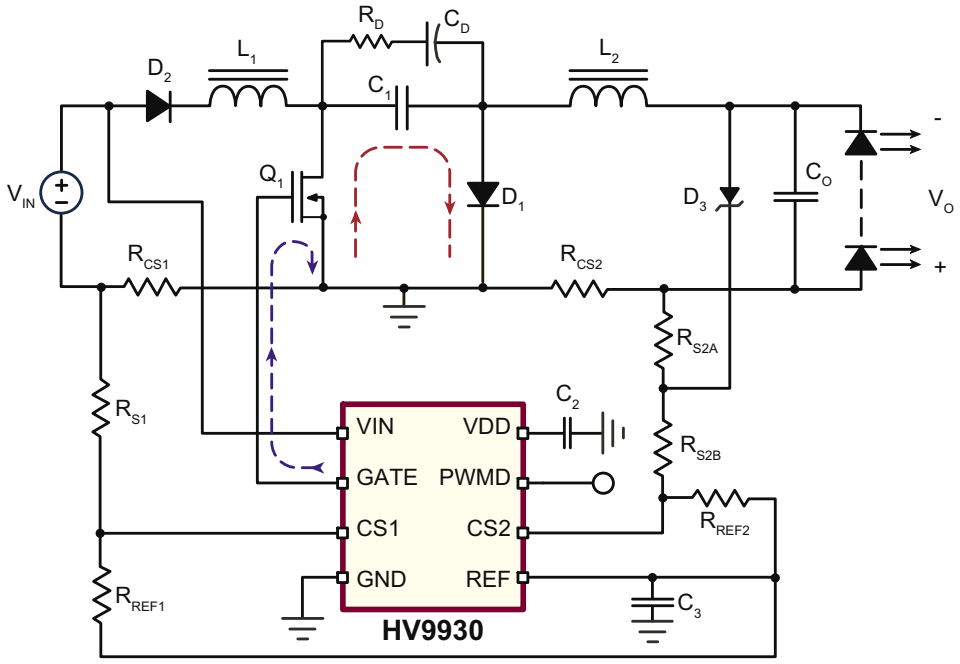

Figure 1-3. EMI Compliance for the HV9930 Based LED Driver

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