MD1213 + TC6320 Demoboard
High Speed ±100V 2A Pulser

General Description

The MD1213DB1 can drive a transducer as a single channel transmitter for ultrasound and other applications. The demoboard consists of one MD1213 in a 12-Lead 4x4x0.9mm QFN (K6) package, combined with Supertex's TC6320, an IC containing high voltage P- and N- channel FETs in a 8-Lead SOIC package.

Logic control inputs INA, INB and OE of the MD1213 are controlled via the six-pin head connector on the board. Due to the fast signal rise and fall time requirement, every ground wire of the ribbon cable must be used to connect from the logic signal source. When OE is enabled, it should recieve the same voltage as the logic source circuit's power supply.

The MD1213DB1 output waveforms can be displayed directly using an oscilloscope by connecting the scope probe to the test point TP10-1 and TP10-2 (GND). The J5 jumper can select whether or not to connect the on-board equivalent-load, a 220pF 200V capacitor paralleled with a 1.0kΩ, 1W resistor. Also, a coaxial cable can be used to easily connect to the user's transducer.

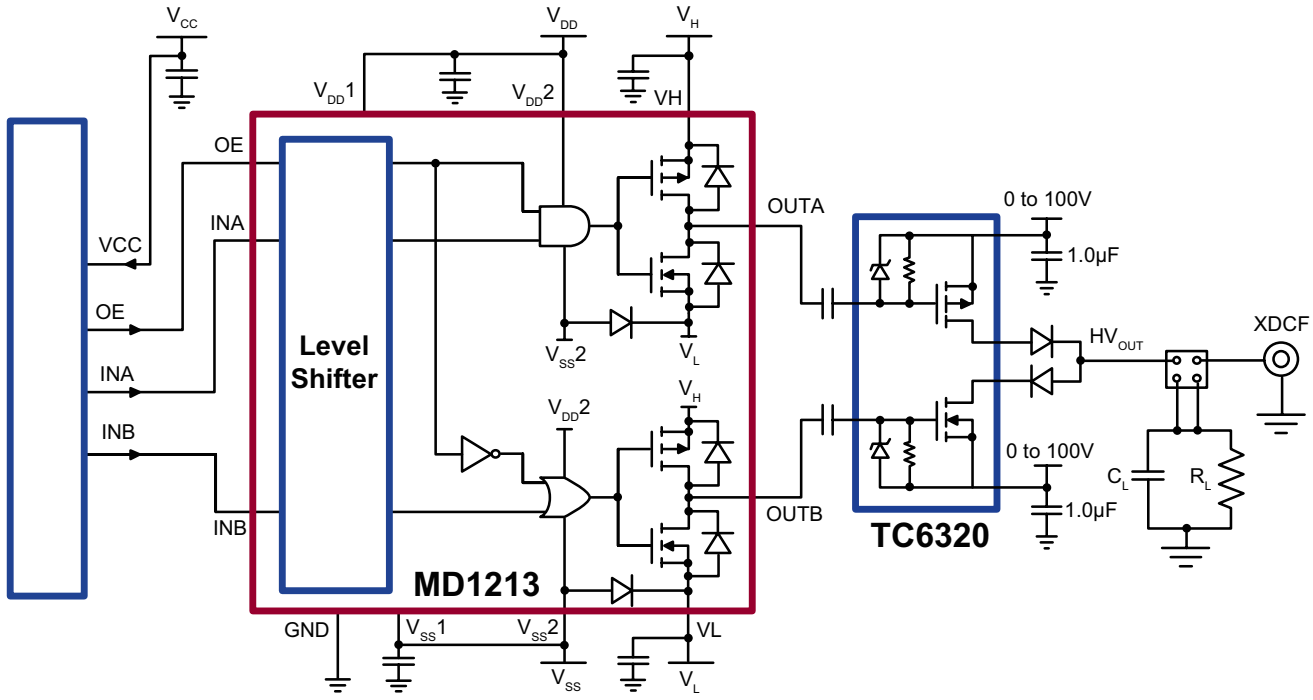
Demoboard Features

- Demonstrates one channel ultrasound transmitter
- MD1213 driving a TC6320 power MOSFET
- ±2.0 A source and sink current capability
- Logic control signal input connector
- SMA connectors for cable to a transducer
- 1.8 to 3.3V CMOS logic interface

Designing a Pulser with the MD1213

Low input capacitance and fast switching speed are the important features of the MD1213's input stage. Its logic inputs have an input impedance of about 20kΩ in parallel with 5pF, and an internal speed of around 100MHz. The output enable pin, OE, determines the threshold voltage for the input-channel level translators. The MD1213's input stage logic is fully compatible with 1.8V, 2.0V, 2.5V, 3.3V, or 5.0V CMOS logic. The level translators are also compatible with these logic voltage levels right up to the MOSFET's gate-driver voltage level, which is typically 5.0V to 12V. When OE is low, the chip disables its' outputs, setting OUTA high and OUTB low. This condition helps to properly pre-charge the AC coupling capacitors that the user can optionally add in series with the gate-driver circuit of the external P/N-channel FET pair.

Block Diagram



Designing a Pulser with the MD1213 *(cont.)*

The MD1213's output stage has separate power pins that enable users to select the output signal's high and low levels independently from the supply voltages that the main part of the circuit uses. For example, the input logic levels could be 0V and 3.3V, and the output levels may lie anywhere in the range of ±5.0V.

Typically, the MD1213's output has rise and fall times of about 6.0ns when driving a 1000pF load. The output stage is capable of peak currents of up to ±2.0A, depending on the system's supply voltages and load capacitance. Such high currents are necessary to drive the input capacitances of the output MOSFETs for fast switching speeds.

The bottom of the MD1213 12-Lead QFN package has a thermal pad for power dissipation enhancement. It must externally connect to the VSS pin on the PCB. This pad is connected internally to the substrate of the IC circuit. It must have the lowest potential voltage of the circuit at all times, including during the power up or down periods, or it could cause circuit latch-up or damage.

The Supertex TC6320 is comprised of an N- and P-channel MOSFET pair with low threshold voltages (2.0V maximum). This 8-Lead SO packaged device features 200V breakdown voltage, 2.0A peak current output capabilities, and low input capacitance (110pF maximum). The TC6320 integrates the gate-source resistors and Zener diodes that a high voltage pulse-driver requires. The high output current capability of the TC6320 MOSFET speeds output waveform rise and fall time, while their low input capacitance minimizes propagation delays.

During power up/down conditions, the high voltage supplies V_{PP} and V_{NN} can inject transient voltages greater than 20V via the output transistor's parasitic gate-to-source capacitances. The maximum permissible gate-to-source voltage (V_{GS}) is ±20V. The TC6320's integral 15 - 18V Zener diodes across its' gate and source terminals protect against such transient voltages. But even if it is possible to slowly ramp the high voltage supplies, these Zener diodes are still crucial, as they also serve as the DC voltage restoration stage for the gates.

Note that it is possible to vary the V_{PP} and V_{NN} voltages without making significant changes to the circuit configuration. For example, V_{NN} can be 0V and V_{PP} +200V for positive unipolar pulses. Or V_{NN} can be -200V and V_{PP} 0V for a negative unipolar pulser. If the user plans to operate the demoboard above 100V, he must adjust the bypass capacitors (C8 or C16) to a voltage rating of 200V. Due to the BV limitation of the TC6320, the differential voltage (V_{PP}-V_{NN}) must not be greater then 200V.

Operating Supply Voltages

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{SS}	Negative drive supply	-5.5	0	0	V	(V_{DD} - V_{SS}) ≤ 13
V_L		V_{SS}	-	V_{DD} -2.0		
V_{DD}	Positive drive supply	4.5	10	12	V	(V_{DD} - V_{SS}) ≤ 13
V_H		V_{SS} +2.0	10	V_{DD}		
V_{CC}	Logic supply	1.8	3.3	5.5	V	---
V_{PP}	TC6320 HV positive supply	0	-	100	V	---
V_{NN}	TC6320 HV negative supply	-100	-	0	V	---

Current Consumption

Symbol	Typ	Units	Conditions
I_{DD}	0.7	mA	V_{DD} = 12V
I_{H}	0.7	mA	V_{H} = 12V
I_{CC}	58	mA	V_{CC} = 3.3V
I_{PP}	2.4	mA	V_{PP} = 100V
I_{NN}	2.5	mA	V_{NN} = -100V

Waveform C, 20MHz, 8 cycles, V_{SS} = V_{L} = 0 Load: 220pF//1.0k

Voltage Supply Power-Up Sequence

1	V_{CC}	Logic voltage supply, and all OE = INA = INB = Low
2	V_{DD}	Positive drive voltage for V_{DD}1,2
3	V_{SS}	0 or -5.0V negative bias voltage for V_{SS}1,2 and IC substrate voltage
4	V_{L}	0 to -5.0V or V_{SS} negative driver voltage for V_{L}
5	V_{H}	0 to +10 or V_{DD} positive driver voltage for V_{H}
6	V_{PP}/V_{NN}	+/-HV supply, slew rate not exceed 2.0V/ms

Note:
The power-down sequence should be the reverse of the power-up sequence above

Board Connector and Test Pin Description

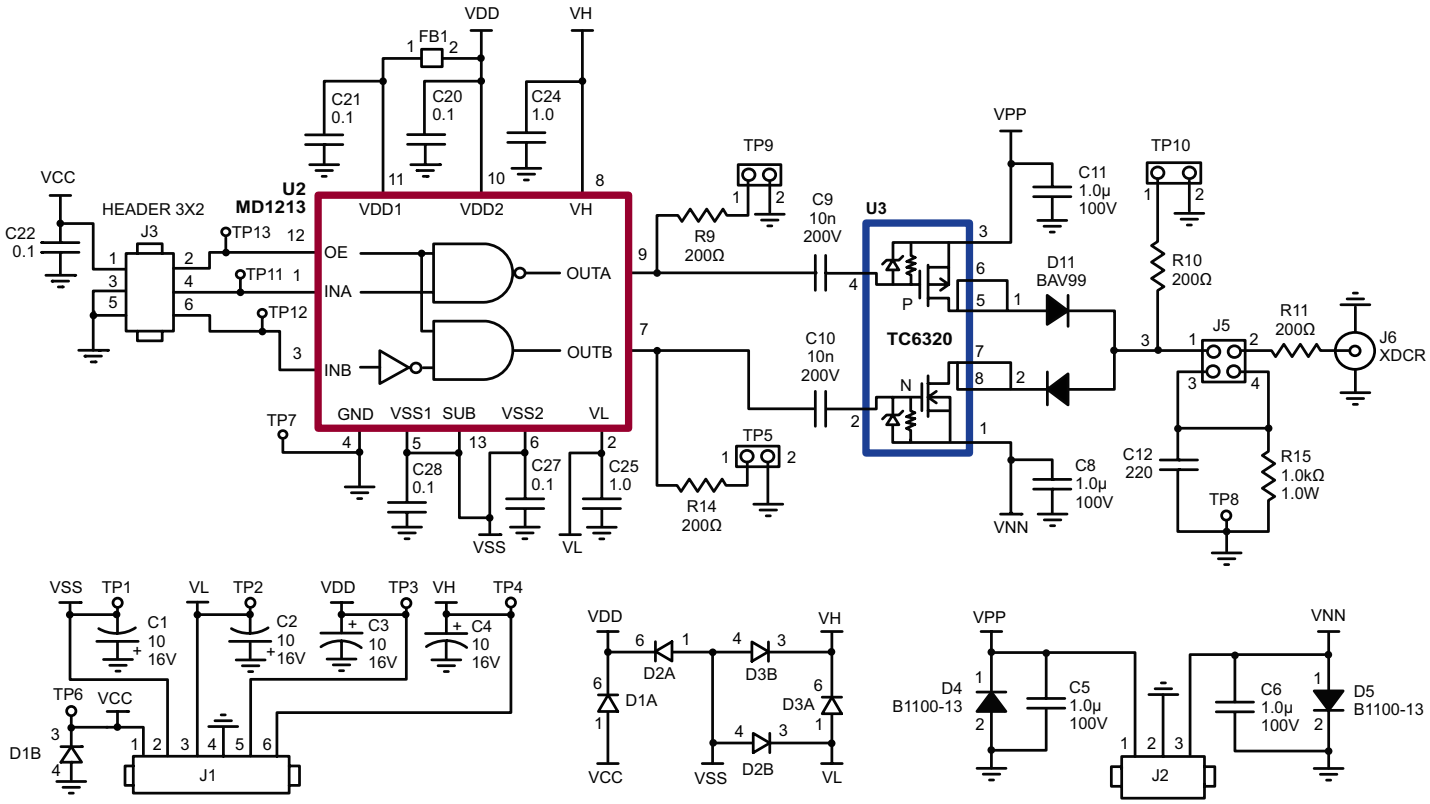
Logic Control Signal Input Connector

Pin	Name	Description
J3-1	VCC	Logic voltage supply for VCC
J3-2	OE	MD1213 OE signal for pulser output enable, when OE=0, TC6320 P and N MOSFET both off.
J3-3	GND	Logic ground
J3-4	INA	---
J3-5	GND	Logic ground
J3-6	INB	---

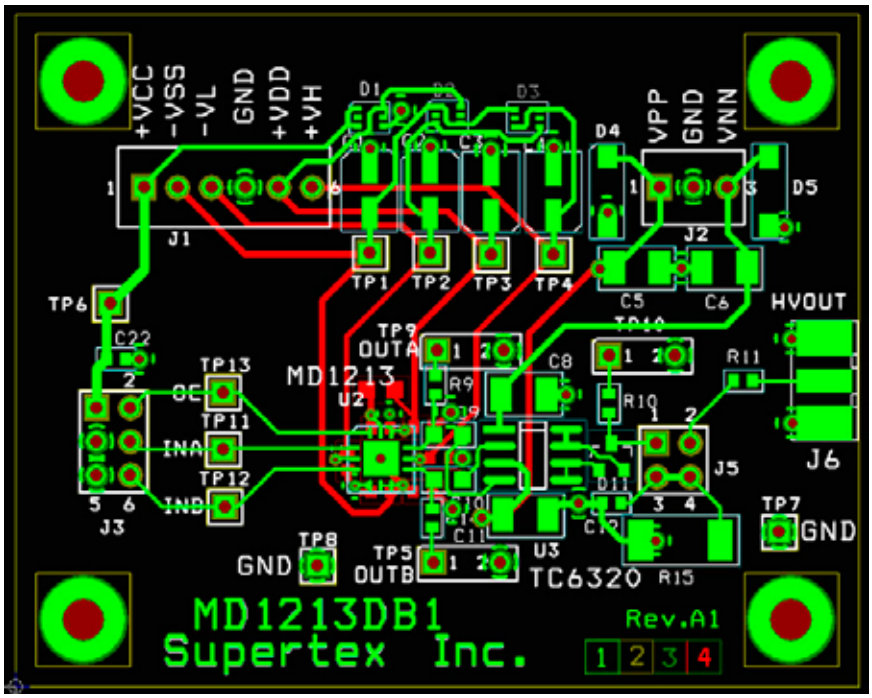
Power Supply Connector

Pin	Name	Description
J1-1	VCC	+3.3 logic voltage supply for V_{CC}
J1-2	VSS	0 or -5.0V negative bias supply for V_{SS}1, V_{SS}2 and SUB
J1-3	VL	0 or -5.0V negative voltage supply for driver output stage
J1-4	GND	Power supply ground
J1-5	VDD	+10V positive driver voltage supply for V_{DD}1 and V_{DD}2
J1-6	VH	+10 or +5.0V positive voltage supply for driver output stage
J2-1	VP_{P}	0 to +100V positive high voltage supply with current limiting maximum to 2.0A
J2-2	GND	High voltage power supply return, 0V
J2-3	VVV	0 to -100V Negative high voltage supply with current limiting maximum to -2.0A

Schematic Diagram



PCB Layout



MD1213DB1 Waveforms

Fig 1: INA, INB, OUTA, OUTB and HV_{OUT} with 220pF//1K Load, V_{DD}= V_H=+12V, V_{SS}= V_L= 0V, V_{PP}/V_{NN}= +/-100V, 10MHz

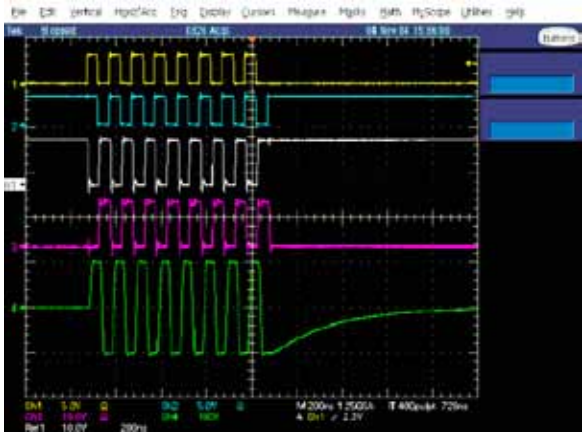
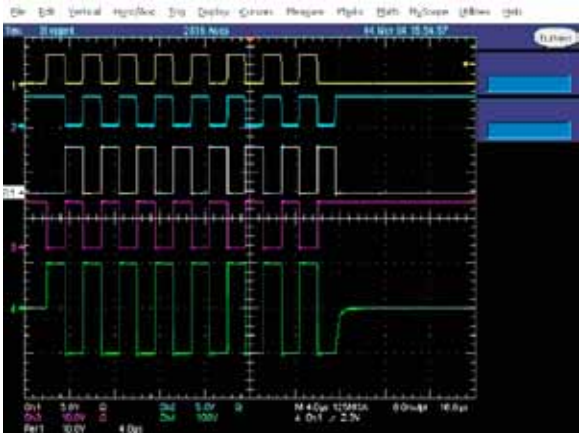


Fig 2: INA, INB, OUTA, OUTB and HV_{OUT} with 220pF//1K Load, V_{DD}= V_H= +12V, V_{SS}= V_L= 0V, V_{PP}/V_{NN}= +/-100V, 20MHz

Fig 3 :INA, INB, OUTA, OUTB and HV_{OUT} with 220pF//1K Load, V_{DD}= V_H=+12V, V_{SS}= V_L= 0V, V_{PP}/V_{NN}= +/-100V, 312.5kHz



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