150V, 1.5A, Unipolar Ultrasound Pulser Demoboard

General Description

The HV7355 is a monolithic eight-channel, high-speed, high voltage, unipolar ultrasound transmitter pulser. This integrated, high performance circuit is in a single, 8x8x0.9mm, 56-lead QFN package.

The HV7355 can deliver guaranteed ±1.5A source and sink current to a capacitive transducer with 0 to +150V peak voltage. It is designed for medical ultrasound imaging and ultrasound material NDT applications. It can also be used as a high voltage driver for other piezoelectric or capacitive MEMS transducers, or for ATE systems and pulse signal generators as a signal source.

The HV7355's circuitry consists of controller logic circuits, level translators, gate driving buffers and a high current and high voltage MOSFET output stage. The output stages of each channel are designed to provide peak output currents typically over ±1.5A for pulsing, with up to 150V swings. The upper limit frequency of the pulser waveform is dependent upon the load capacitance. With different capacitance load conditions the maximum output frequency is about 20MHz.

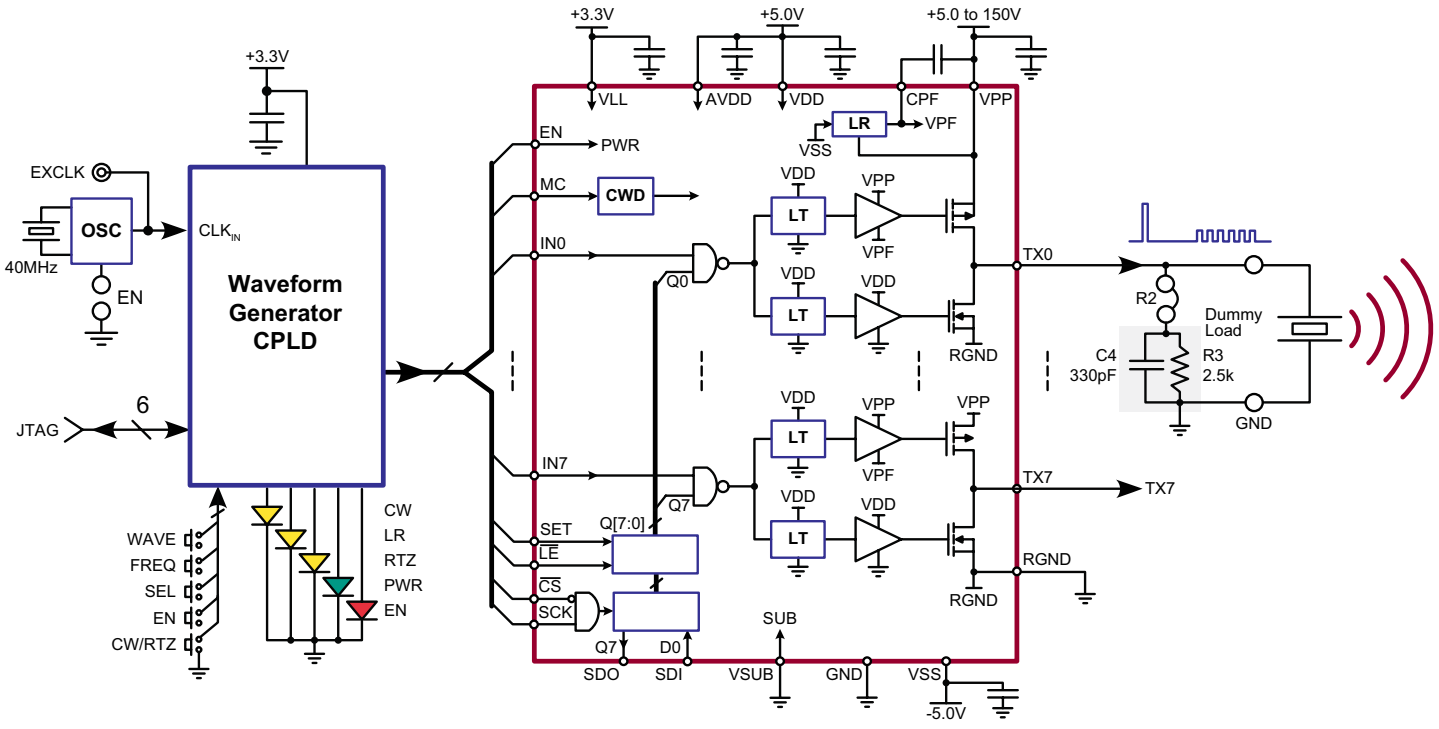
This demoboard datasheet describes how to use the HV7355DB1 to generate the basic high voltage pulse waveform as an ultrasound transmitting pulser.

The HV7355 circuit uses DC-coupling from a 3.3V logic input to output TX0~7 internally, therefore the chip needs three sets of voltage supply rails: V_{LL} (+3.3V), V_{DD}/V_{SS} (+/-5.0V) and V_{PP} (up to +150V). The V_{PP} high voltage supply can be changed rather quickly, compared to the capacitor gate-coupled driving pulsers. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

The control signal logic-high voltage should be the same as the V_{LL} voltage of the IC, and the logic-low should be referenced to GND.

The HV7355DB1 output waveforms can be displayed using an oscilloscope by connecting the scope probe to the test points TX0~7 and GND. The soldering jumper can select whether or not to connect the on-board dummy load, a 330pF capacitor paralleling with a 2.5kΩ resistor. The test points can be used to connect the user's transducer to easily evaluate the pulser.

Block Diagram



The PCB Layout Techniques

The large thermal pad at the bottom of the HV7355 package is internally connected to the IC's substrate (VSUB). This thermal pad should be connected to 0V or GND externally on the PCB. The designer needs to pay attention to the connecting traces on the outputs TX0~7, as the high-voltage and high-speed traces. In particular, controlled-impedance to the ground plane and more trace spacing needs to be applied in this situation.

High-speed PCB trace design practices that are compatible with about 50 to 100MHz operating speeds are used for the demo board PCB layout. The internal circuitry of the HV7355 can operate at quite a high frequency, with the primary speed limitation being load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors and the driver to the FET's gate-coupling capacitors should be as close to the pins as possible. The GND pin should have low inductance feed-through via connections that are connected directly to a solid ground plane. The VDD, VSS, VPP and CPP voltage-supply and/or bypass capacitor pins can draw fast transient currents of up to 2.0A, so they should be provided with a low-impedance bypass capacitor at the chip's pins. A ceramic capacitor of 1.0 to 2.0µF may be used. Only VPP to GND capacitors need be high voltage. CPF to VPP capacitors only need be low voltage. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. For applications that are sensitive to jitter and noise when using multiple HV7355 ICs, insert another ferrite bead between each chips supply line.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of the HV7355's high voltage power stages is very low, to obtain better waveform integrity at the load terminals after long cables, in some cases it may be desirable to add a small value resistor in series with the outputs TX0~7. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Be aware of the parasitic coupling from the outputs to the input signal terminals of the HV7355.

This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 3.3V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

Testing the Integrated Pulser

The HV7355 pulser demoboard should be powered up with a DC power supplie that has current limiting functions.

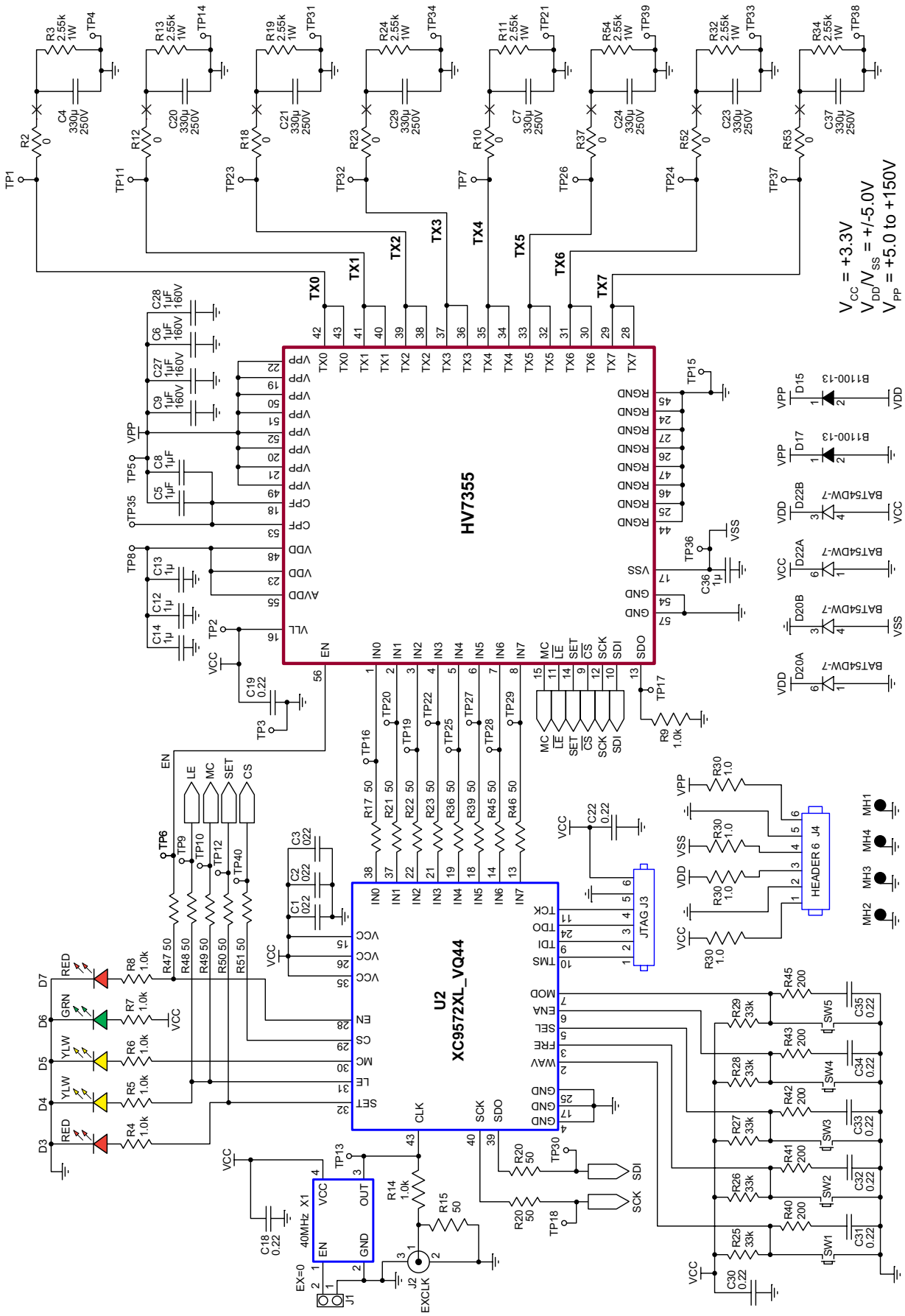
To meet the typical loading conditions, the on-board dummy load 330pF//2.5kΩ should be connected to the high voltage pulser output through the solder jumper when using an oscilloscope's high impedance probe. To evaluate different loading conditions, the values of the RC within the current and power limit of the device may be changed.

In order to drive the user's piezo transducers with a cable, one should match the output load impendence properly to avoid cable and transducer reflections. A 70 to 75Ω coaxial cable is recommended. The coaxial cable end should be soldered to TX0~7 and GND directly with very short leads. If a user's load is being used, the on-board dummy load should be disconnected by cutting the small shorting copper trace in between the zeroΩ resistor's (R2, R12 etc.) pads. They are shorted by factory default.

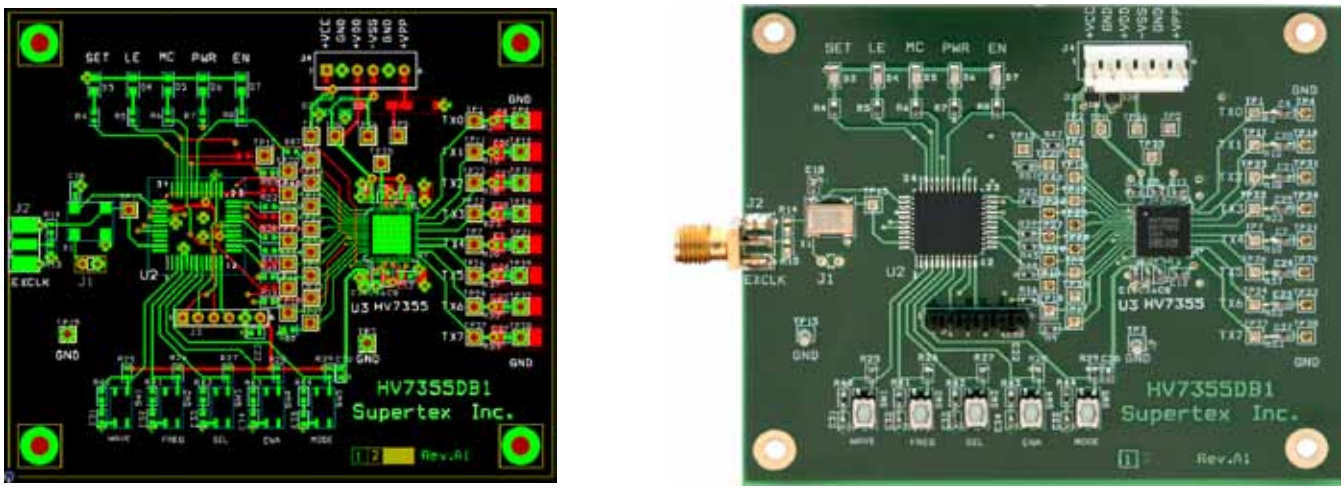
All of the on-board test points are designed to work with the high impedance probe of the oscilloscope. Some probes may have limited input voltage. When using the probe on these high voltage test-points, make sure that V_{PP} voltages do not exceed the probe limit. Using the high impendence oscilloscope probe for the on-board test points, it is important to have short ground leads to the circuit board ground plane.

Precautions need to be applied to not overlap the logic-high time periods of the control signals. Otherwise, permanent damage to the device may occur when cross-conduction or shoot-through currents exceed the device's maximum limits.

HV7355DB1 Schematic



HV7355DB1 PCB and Board Layout



Actual Board Size: 72.4mm x 68.4mm

Power Connector Description

1	V_{CC}	+3.3V Logic voltage input for V_{LL} and CPLD. (100mA)
2	GND	0V, Ground
3	V_{DD}	+5.0V HV7355 positive V_{DD} supply. (25mA)
4	V_{SS}	-5.0V HV7355 negative V_{SS} supply. (-25mA)
5	GND	0V, Ground
6	V_{PP}	+10 to +150V positive high voltage supply. (5mA)

Voltage Supply Power-Up and Operation Sequence

1	$+V_{CC}$	+3.3V positive logic supply voltage for HV7355's V_{LL} and CPLD V_{CC}.
2	$+V_{DD}$ / $-V_{SS}$	±5.0V positive and negative V_{DD} and V_{SS} power supply.
3	$+V_{PP}$	+10 to +150V positive high voltage.

Note:
Power-down in reverse order

Push Button Operations

WAV	Toggle select pulse B-mode waveforms: None, 1-cycle, 3-cycles, 7-cycles.
FREQ	Toggle select frequency: 20, 10, 5, 2.5, 1.25 and 0.625MHz when X1 oscillator is 40MHz.
SEL	Toggle select. Increases the off-time between 2 consecutive pulses.
EN	Toggle ON or OFF HV7355 chip enable
MODE	Toggle select between B-mode and CW.

LED Indicator

SET	Set the latch registers of serial interface, when high, all latches are set to logic high.
$\overline{LE}$	Latch enable when low, data can be latched into the registers of serial interface.
MC	Mode control, high indicates B-mode and low indicates CW.
PWR	HV7355 V_{LL} 3.3V and CPLD chip V_{CC} power supply indicator.
EN	HV7355 chip enable signal indicator. Power state initially is OFF until EN is pushed.

Typical Waveforms

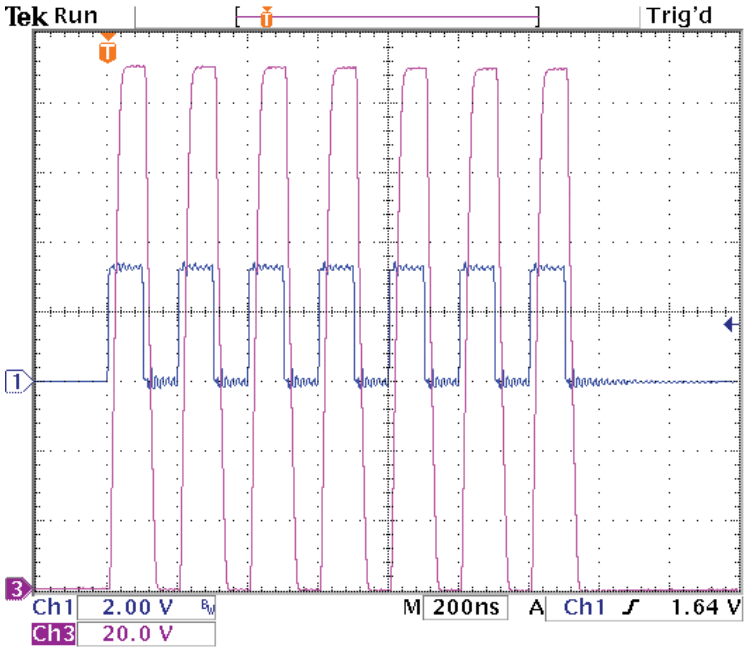


Figure 1. Input logic and TX output waveforms of 5.0MHz (0 to +150V with 330pF//2.5kΩ load)

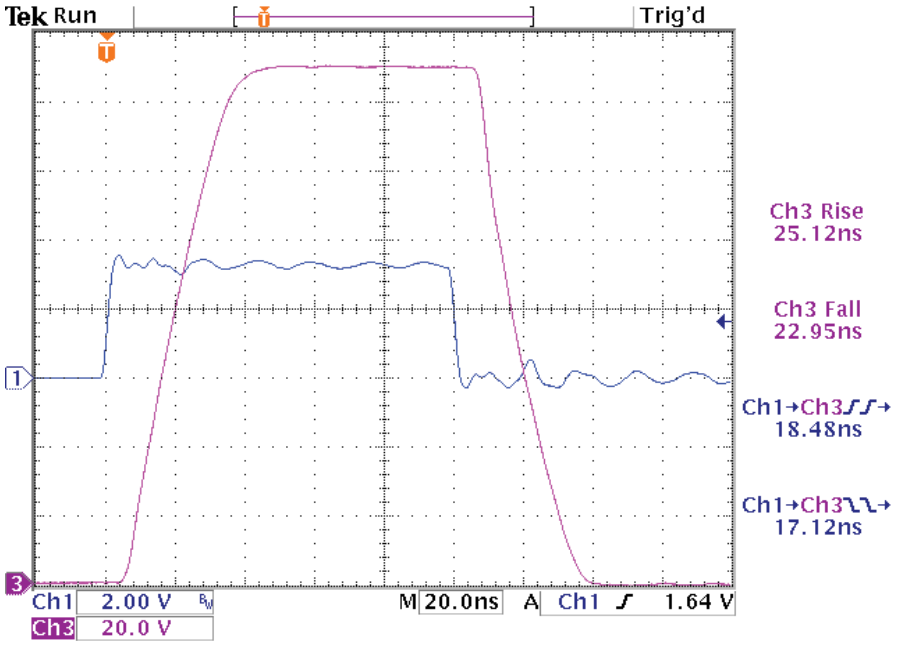


Figure 2. Rise and fall time at 0 to +150V (with 330pF//2.5kΩ load)

Typical Waveforms *(cont.)*

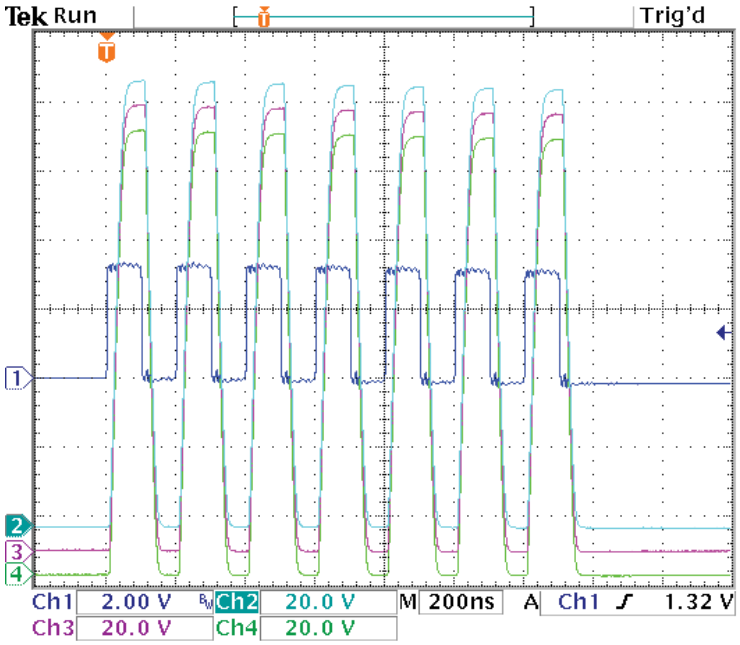


Figure 3. Multiple channel at 5.0MHz (0 to +150V with 330pF//2.5kΩ load)

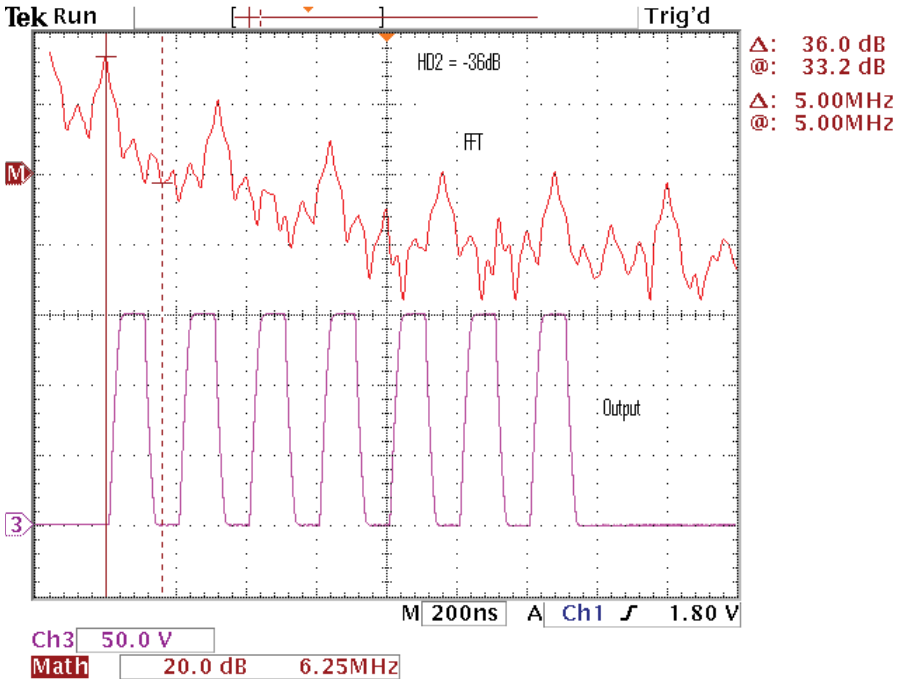


Figure 4. FFT Plot of Second Harmonic Distortion (HD2) -36dB at 5.0MHz, V_{PP} = 150V (with 330pF//2.5kΩ load)

Typical Waveforms *(cont.)*

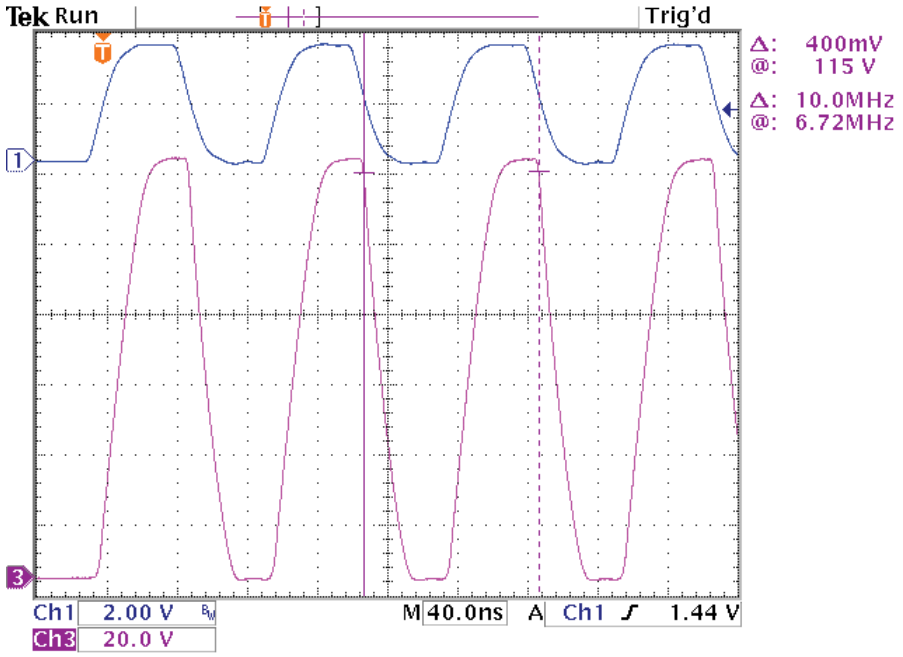


Figure 5. Output Waveform at 10MHz and V_{PP} = 120V (with 330pF//2.5kΩ load)

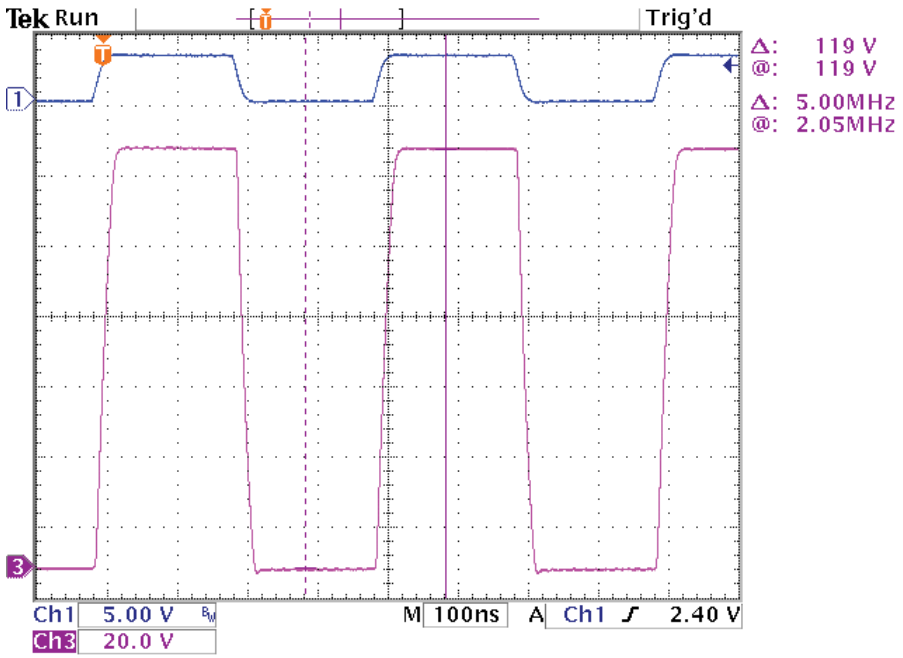


Figure 6. Output Waveform at 2.5MHz and V_{PP} = 120V (with 330pF//2.5kΩ load)

Typical Waveforms *(cont.)*

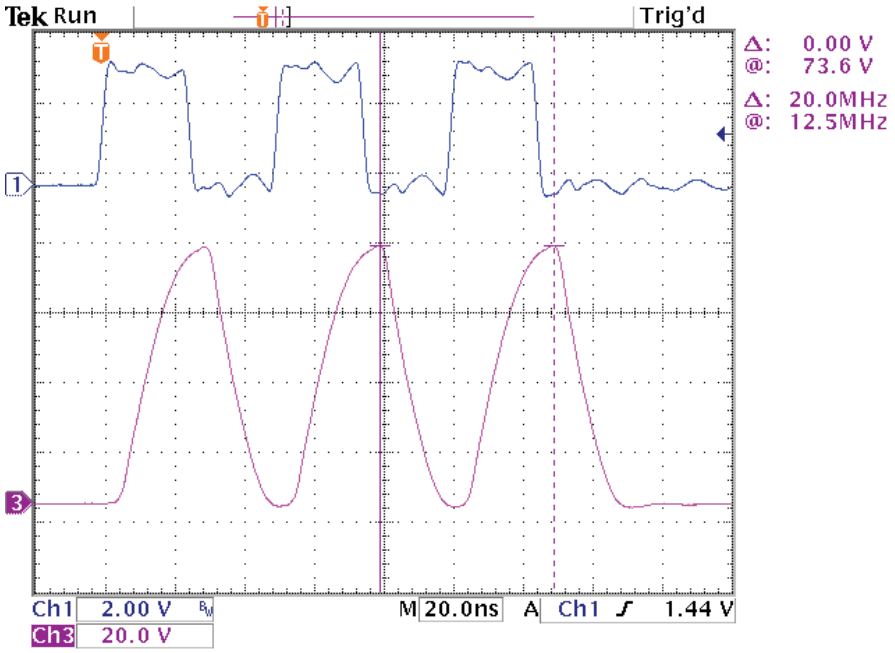


Figure 7. Output Waveform at 20MHz at V_{PP} = 75V (with 330pF//2.5kΩ load)

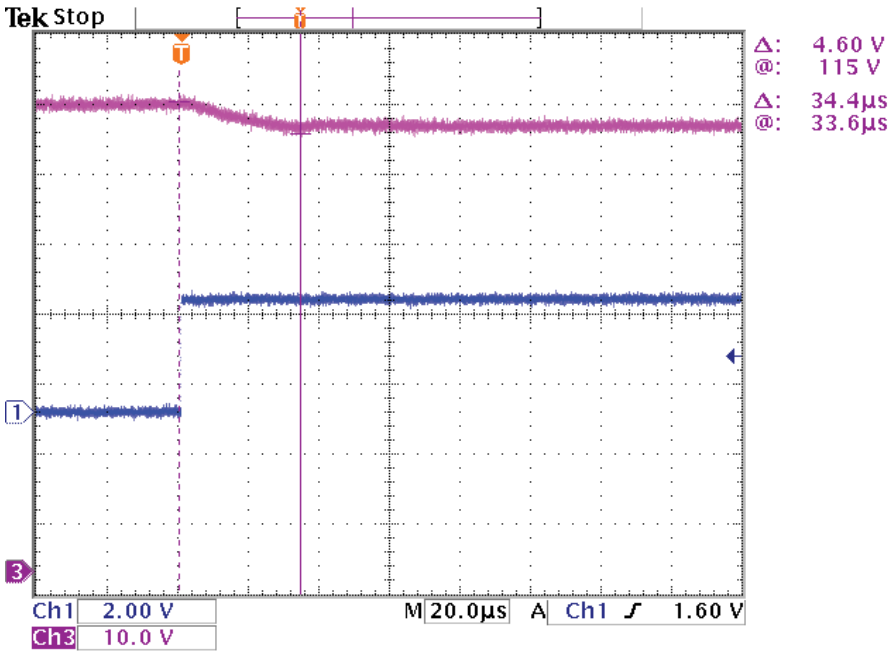


Figure 8. Power on EN chip enable to VPF setting time

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