

## Six Pair, N- and P-Channel Enhancement-Mode MOSFET

### Features

- ▶ Six N- and P-channel MOSFET pairs
- ▶ Integrated gate-to-source resistor
- ▶ Integrated gate-to-source Zener diode
- ▶ Low threshold
- ▶ Low on-resistance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

### Applications

- ▶ High voltage pulsers
- ▶ Amplifiers
- ▶ Buffers
- ▶ Piezoelectric transducer drivers
- ▶ General purpose line drivers
- ▶ Logic level interfaces

### General Description

The Supertex TC7320 consists of a six pairs of high voltage, low threshold, N- and P-channel MOSFETs in a 32-lead LQFP package. All of the MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high voltage pulser applications. This low threshold, enhancement-mode (normally-off), transistor utilizes an advanced lateral DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's lateral DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

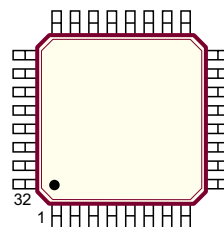
### Ordering Information

Device	32-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.80mm pitch	$BV_{DSS}/BV_{DGS}$ (V)		$R_{DS(ON)}$ (max) ( $\Omega$ )	
		N-Channel	P-Channel	N-Channel	P-Channel
TC7320	TC7320FG-G	200	-200	20	20

-G indicates package is RoHS compliant ('Green')



### Pin Configuration



32-Lead LQFP (FG)

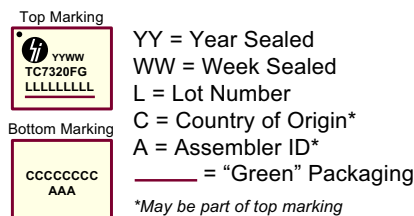
### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C
Power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Package Marking



Package may or may not include the following marks: Si or

32-Lead LQFP (FG)

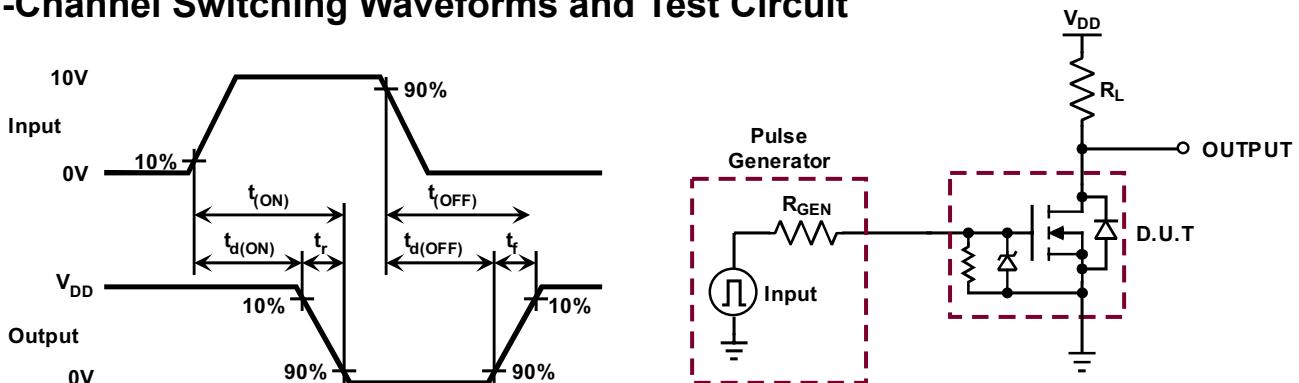
**N-Channel Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	200	-	-	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate threshold voltage	-	0.4	-	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
$R_{GS}$	Gate-to-source shunt resistor	0.8	-	2.0	K $\Omega$	$I_{GS} = 100\mu A$
$\Delta R_{GS}$	Change in $R_{GS}$ with temperature	-	-7.5	-	%/°C	$I_{GS} = 100\mu A$
$VZ_{GS}$	Gate-to-source Zener voltage	10	-	18	V	$I_{GS} = 2.0mA$
$\Delta VZ_{GS}$	Change in $VZ_{GS}$ with temperature	-	-0.5	-	mV/°C	$I_{GS} = 2.0mA$
$I_{DSS}$	Zero gate voltage drain current	-	-	10.0	$\mu A$	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	1.0	-	-	A	$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	20	$\Omega$	$V_{GS} = 10V, I_D = 150mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.6	1.0	%/°C	$V_{GS} = 10V, I_D = 150mA$
$G_{FS}$	Forward transconductance	-	150	-	mmho	$V_{DS} = 25V, I_D = 200mA$
$C_{ISS}$	Input capacitance	-	-	150	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	-	75		
$C_{RSS}$	Reverse transfer capacitance	-	-	25		
$t_{d(ON)}$	Turn-on delay time	-	-	12	ns	$V_{DD} = 25V, I_D = 500mA, R_{GEN} = 25\Omega$
$t_r$	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	25		
$t_f$	Fall time	-	-	40		
$V_{SD}$	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 500mA$
$t_{rr}$	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

**Notes:**

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu$ s pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

**N-Channel Switching Waveforms and Test Circuit**



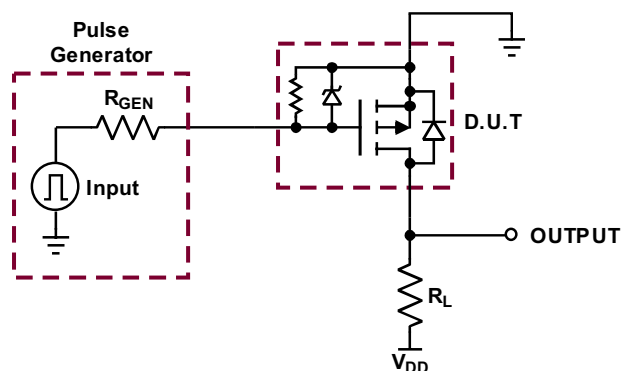
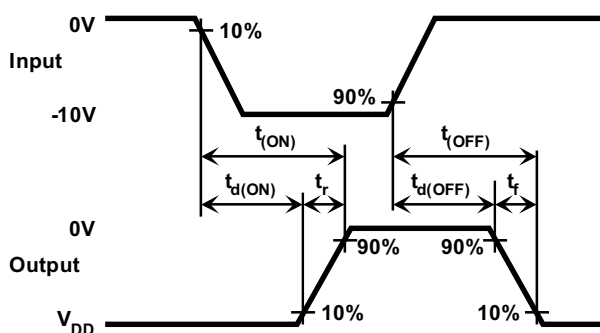
**P-Channel Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	-200	-	-	V	$V_{GS} = 0V, I_D = -1.0mA$
$V_{GS(th)}$	Gate threshold voltage	-	-2.3	-	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	$V_{GS} = V_{DS}, I_D = -1.0mA$
$R_{GS}$	Gate-to-source shunt resistor	0.8	-	2.0	K $\Omega$	$I_{GS} = -100\mu A$
$\Delta R_{GS}$	Change in $R_{GS}$ with temperature	-	-7.5	-	%/°C	$I_{GS} = -100\mu A$
$VZ_{GS}$	Gate-to-source Zener voltage	10	-	18	V	$I_{GS} = -2.0mA$
$\Delta Z_{GS}$	Change in $VZ_{GS}$ with temperature	-	-0.5	-	mV/°C	$I_{GS} = -2.0mA$
$I_{DSS}$	Zero gate voltage drain current	-	-	-10	$\mu A$	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-1.0	-	-	A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	20	$\Omega$	$V_{GS} = -10V, I_D = -150mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.6	1.0	%/°C	$V_{GS} = -10V, I_D = -150mA$
$G_{FS}$	Forward transconductance	-	150	-	mmho	$V_{DS} = -25V, I_D = -200mA$
$C_{ISS}$	Input capacitance	-	-	200	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	-	100		
$C_{RSS}$	Reverse transfer capacitance	-	-	35		
$t_{d(ON)}$	Turn-on delay time	-	-	15	ns	$V_{DD} = -25V, I_D = -500mA, R_{GEN} = 25\Omega$
$t_r$	Rise time	-	-	20		
$t_{d(OFF)}$	Turn-off delay time	-	-	35		
$t_f$	Fall time	-	-	30		
$V_{SD}$	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -500A$
$t_{rr}$	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -500A$

**Notes:**

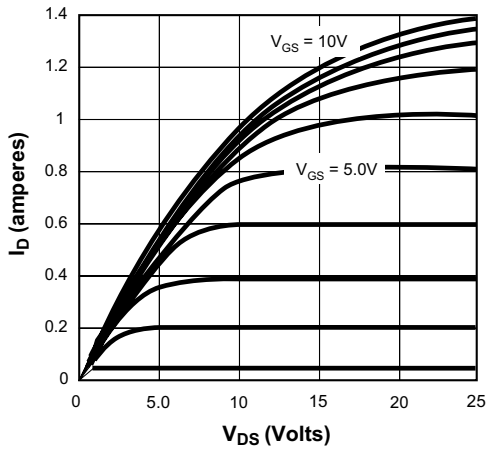
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu s$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

**P-Channel Switching Waveforms and Test Circuit**

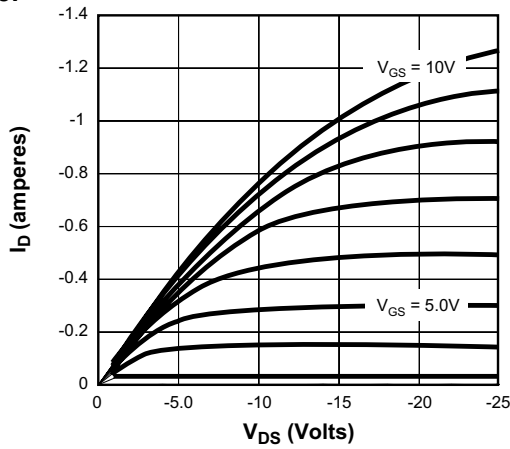


Typical I-V Characteristics

N-Channel



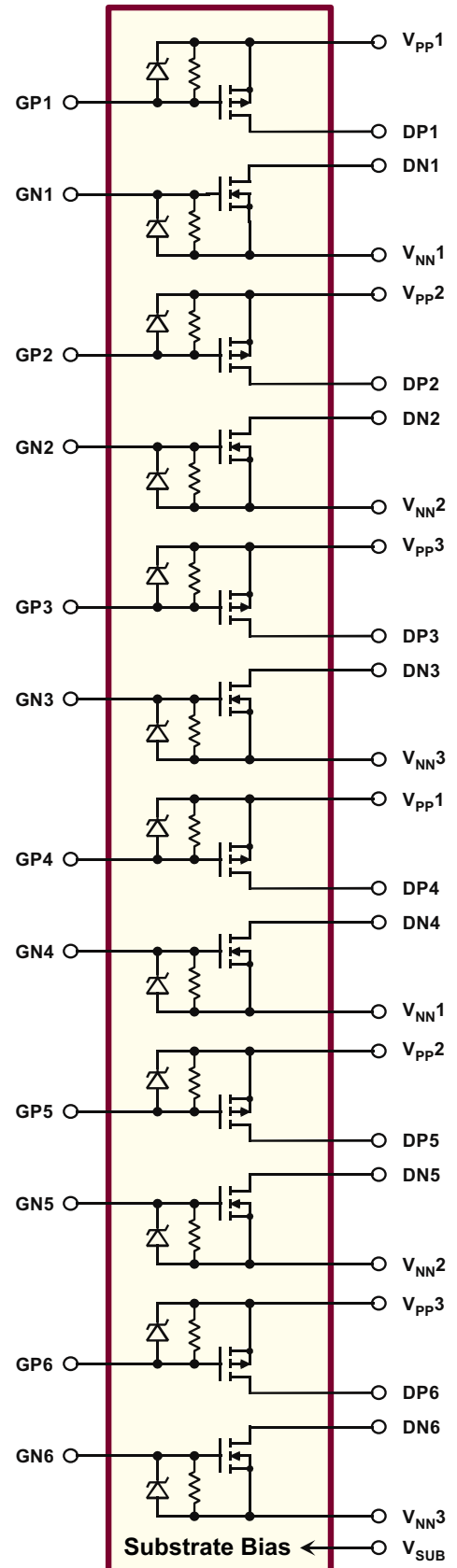
P-Channel



Pin Descriptions

Pin #	Function	Pin #	Function
1	GP1	17	DN6
2	GN1	18	DN3
3	GN2	19	DN5
4	GN3	20	N/C
5	GN6	21	V <sub>NN2</sub>
6	GN5	22	DN2
7	GN4	23	DN4
8	GP4	24	DN1
9	GP5	25	V <sub>NN1</sub>
10	GP6	26	V <sub>PP1</sub>
11	DP6	27	DP1
12	V <sub>PP2</sub>	28	DP2
13	DP5	29	V <sub>PP3</sub>
14	DP4	30	DP3
15	V <sub>SUB</sub> *	31	GP3
16	V <sub>NN3</sub>	32	GP2

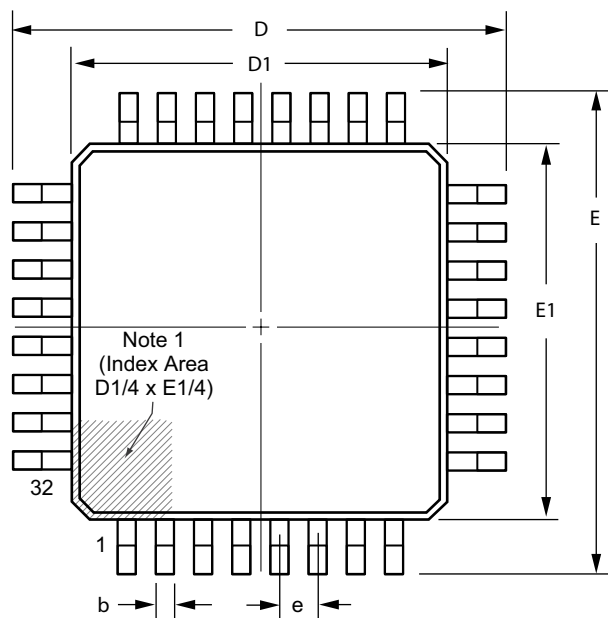
Block Diagram



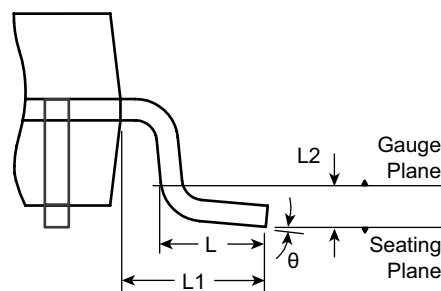
\* The V<sub>SUB</sub> pin needs to be connected to the most positive supply

# 32-Lead LQFP Package Outline (FG)

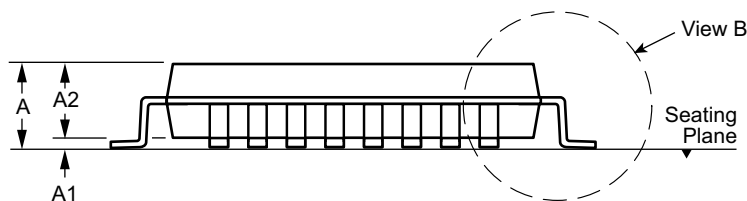
7.00x7.00mm body, 1.60mm height (max), 0.80mm pitch



**Top View**



**View B**



**Side View**

**Note:**  
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	
Dimension (mm)	MIN	1.40*	0.05	1.35	0.30	8.80*	6.80*	8.80*	6.80*	0.80 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.37	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.45	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBA, Issue D, Jan. 2001.  
\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.  
Drawings are not to scale.  
Supertex Doc. #: DSPD-32LQFPFG, Version E101708.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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