# MD2134 Ultrasound Beamforming Transmitter Demoboard with Coupled Inductor

#### Introduction

The MD2134 is a high speed, arbitrary waveform, push-pull source driver. It is designed for medical ultrasound imaging and HIFU beamforming applications. It also can be used in NDT, sonar and other ultrasound phase-array focusing beamforming applications.

The MD2134 consists of CMOS digital logic input circuits, an eight-bit current DAC for aperture weighting amplitude control, and a programmable 15-level pulse amplitude modulation (PAM) current-source that does not includes a zero level. The fast current sources are constructed with a current-switch array, controlled by the LV0~LV15 levelregister as the waveform data points. Four logic inputs M[3:0] are used for transmit data level selecting, as well as the transmitting timing control pins. Each level can be programmed to a resolution of +/-127 including zero (8-bit), in addition to an 8-bit SPI apodization DAC. The outputs PA and PB are controlled by M[3:0] pins directly, as well as the polarity-flip bit S1 in the SPI register. The high-speed SPI interface will achieve per-scan-line fast data updating for dynamically changing delay time, weighting and waveforms. These 15 levels can be selected at any time prior to the pulse launch by reprogramming via SPI.

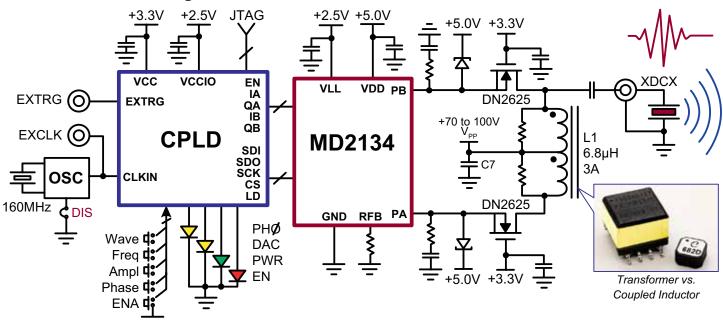
The MD2134 output stage is designed to drive two depletion mode, high voltage, Supertex DN2625 MOSFETs as source drivers. The MOSFET drains are connected to a centertapped or coupled inductor, then to the high voltage supply. One of the DN2625 drains can then be capacitor coupled to the ultrasound transducer piezo load via a cable. The MD2134 has a high speed serial data interface that quickly updates the data register's per-scan-line for changing the beamforming waveforms and apodization amplitudes.

### **General Description**

This MD2134DB2 datasheet describes how the demoboard is to used to generate the ultrasound transmit beamforming waveform with the Gaussian profile, and the adjustable frequency, amplitude and phase angle. It also provides information on how to design a user application circuit and PCB using the Supertex MD2134 and DN2625 devices.

The MD2134DB2 circuit uses two depletion-mode MOSFETs in the push-pull mode to drive the coupled inductor. The two depletion-mode MOSFETs are packaged in a single 5x5mm DFN package. The sources of the MOSFETs are directly driven by the MD2134's two outputs, whose maximum peak sinking current is up to 3.0A. These current source outputs are controlled by the MD2134's internal array-switch of the fast PAM current sources.

### **Demoboard Block Diagram**



On the demoboard the MD2134 logic control signals are generated by two small CPLD programmable logic circuits, clocked by an on-board 160MHz crystal oscillator. The CPLD circuits not only generate accurate timing for the high speed PAM control waveforms, but also the serial data and clock to set and change the waveform amplitude DAC and PAM waveform data registers. An external clock input can be used if the on-board oscillator is disabled. The external trigger input can be used to synchronize the burst waveform launch timing. There are five push buttons for enabling and selecting the output waveform frequency, phase angle and amplitude. Four color LEDs indicate the power, chip enable and wave-form parameter selection states. The MD2134DB2 output waveform can be displayed by using an oscilloscope and the high impedance probe at the TP13 test point. It also can use an SMA to BNC,  $50\Omega$ , coaxial cable to directly connect to an oscilloscope, with an attenuation of 5:1 if R10 is  $200\Omega$ . A cable can also be used to directly drive the user's transducer. Jumper J4 can be used to select whether or not to connect the on-board equivalent load, which is formed by a 220pF capacitor in parallel with a  $1.0k\Omega$  resistor.

#### Circuit Design & PCB Layout

The thermal pad at the bottom of the MD2134 package must be connected to the VSUB pin on the PCB. The VSUB is connected to the IC's substrate. It is important to make sure that the VSUB is well grounded under all conditions. A proper supply voltage power-up sequence is needed to test the circuit. To prevent any supply voltage polarity reversing, the circuit also has the protection of Schottky diodes D7, D8 and D9.

Due to the high current and high current slew rate nature of this common gate, source driven and push-pull circuit topology, the two cascading N-channel MOSFETs need to have very low lead inductance. The DN2625D MOSFET is designed for this application, and works seamlessly with the MD2134. In particular, a good PCB layout design needs to shorten the traces between the MD2134 output pins and DN2625D source pins. It is also necessary to connect all three pairs of pins between them for the high current carrying capacity.

Furthermore, because of the high *di/dt* in the output current of the MD2134, it is also necessary to have the Schottky diodes D5 and D6 from the driver output pins to the +5.0V power supply line as the clamping diodes. Note that the di-

odes must have enough speed and peak current capability. The RC snubber circuits of R8-C5 and R15-C28 at the output pins can effectively dump the current pulse edge ringing.

PCB designers need to pay attention to some of the connecting traces as high voltage and high speed traces. In particular, low capacitance to the ground plane and more trace spacing need to be applied in this situation. High speed PCB trace design practices that are compatible with operating speed of about 100 to 200 MHz are used for the demoboard PCB layout. The internal circuitry of the MD2134 can operate at quite a high frequency, with the primary speed limitation being load capacitance. Because of this high speed, and the high transient currents that result when driving even very small inductive loads, ringing and even oscillations are possible.

The supply voltage bypass capacitors and the MOSFET gate decoupling capacitors should be as close to the pins as possible. The capacitor's ground pin pads should have low inductance feed-through connections that are connected directly to a solid ground plane. The VDD and VPP supplies can draw fast transient currents of up to 3.5A, so they should be provided with a low impedance bypass capacitor at the chip's pins. A ceramic capacitor of 0.1 to 1.0µF may be used. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines.

For applications that use multiple MD2134 ICs and are sensitive to jitter and noise, insert another ferrite bead between the VDD pins, and decouple each chip supply separately. Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance, not only on the supply pins but also on the CA/B and KA/B compensation pins. Very closely placed surface mount components are highly recommended. Be aware of the parasitic coupling from the high voltage outputs to the input signal terminals of the MD2134. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 2.5V, even small coupling voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

This MD2134DB2 beamforming demoboard should be powered up with multiple DC power supplies with current limiting functions. The power supply voltages and current limits used in the testing are listed on page 11. There are examples of the MD2134DB2 demoboard input and output waveforms and measurements shown in Figures 1 to 8.

# Select the Coupled Inductor and Output Capacitor

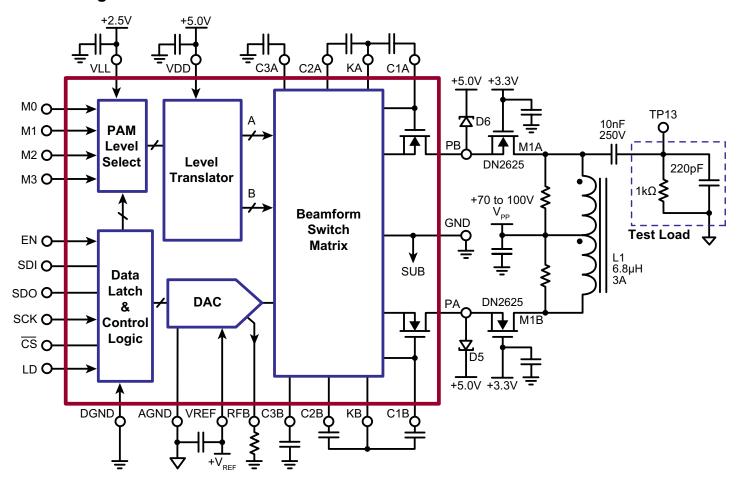
A center-taped or coupled inductor is needed for the push pull output circuit to work. The inductor serves the function of differential current-mirroring between the two DN2625 output drain signals from one arm to the other, very similar to the center-tapped transformer. But the AC coupling and isolation barrier to the ultrasound probe is simply provided by a high voltage 10nF capacitor C40.

The MD2134 PAM signals may operate in the 40 to 160MHz frequency range, however the coupled inductor only needs to work in the frequency band of the ultrasound being transmitted. Beside the bandwidth consideration, the inductor also needs enough peak current capacity and coupling efficiency at RF to make sure the ferrite magnetic core will not be saturated, and has a low leakage inductance. The output coupling capacitor must be high voltage type. In the case of 100V  $V_{\rm pp}$ , a C40 working voltage rating of 200V or higher is necessary.

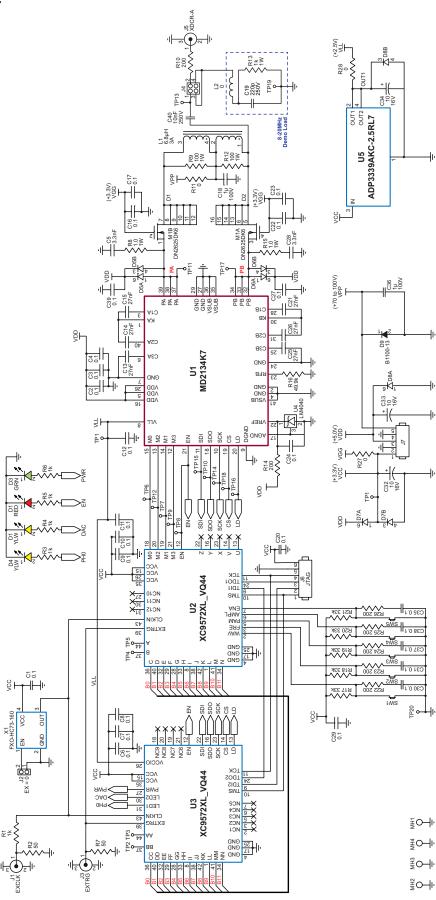
### **Demo Load Emulation Circuitry**

The demo load emulation circuit contains the capacitor C19 (220pF) and the resistor R13 (1.0k). This built-in dummy load emulates a typical wide bandwidth transducer PZT element on the demoboard. It should be disconnected when the user's transducer is connected to the output SMA by the jumper connector J4.

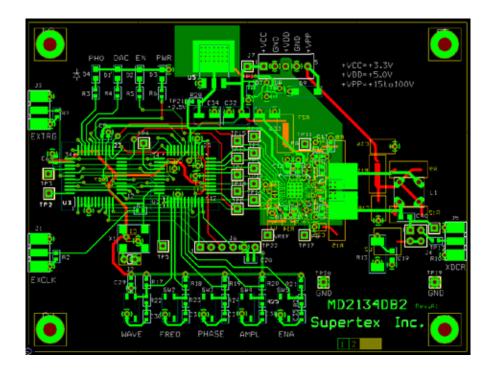
### **Circuit Diagram**



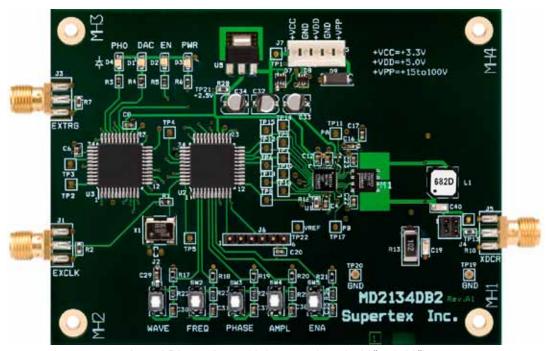
### **Circuit Schematic**



# **PCB Layout**



### MD2134DB2 Demoboard



Actual Dimensions: 10.2cm x 7.6cm (4.00" x 3.00")

# MD2134DB2 Input and Output Waveforms

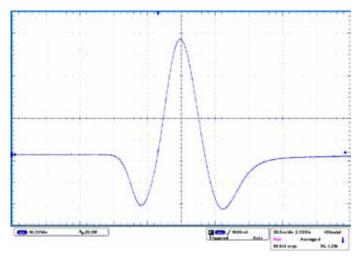


Figure 1: MD2134DB2 8MHz DAC = 127

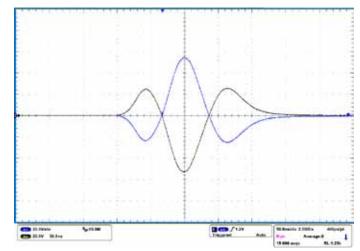


Figure 2: MD2134DB2 8MHz DAC = 127 S1 = 1 & 0

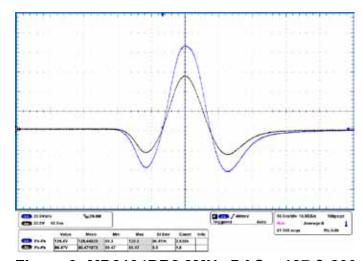


Figure 3: MD2134DB2 8MHz DAC = 127 & 200

# MD2134DB2 Input and Output Waveforms (cont.)

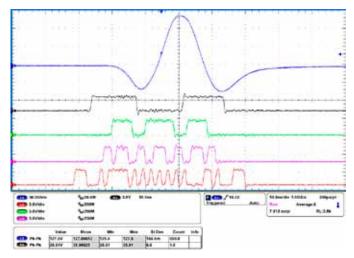


Figure 4: MD2134DB2 8MHz M3-0 & TP13

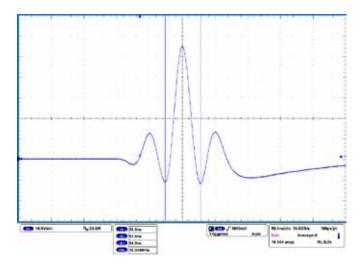


Figure 5: MD2134DB2 20MHz

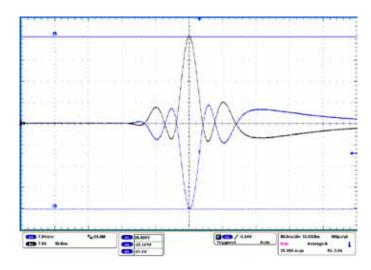


Figure 6: MD2134DB1 20MHz DAC = 127 S1 = 1 & 0

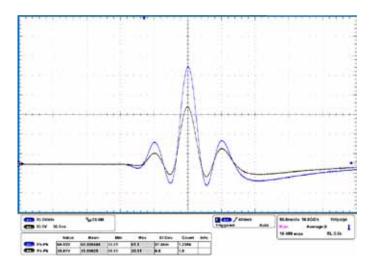


Figure 7: MD2134DB2 20MHz DAC = 127 & 200

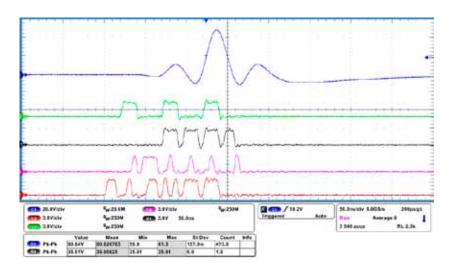


Figure 8: MD2134DB2 20MHz M3-0 & TP13

# **Current Level Control Pin Description**

Input Control Pin Name			е	PAM	Dogovinski ov
М3	M2	M1	M0	Current Level	Description
0	0	0	0	LV0	PA & PB both off, zero current.
0	0	0	1	LV1	Select LV1 current magnitude to PA.
0	0	1	0	LV2	Select LV2 current magnitude to PA.
0	0	1	1	LV3	Select LV3 current magnitude to PA.
0	1	0	0	LV4	Select LV4 current magnitude to PA.
0	1	0	1	LV5	Select LV5 current magnitude to PA.
0	1	1	0	LV6	Select LV6 current magnitude to PA.
0	1	1	1	LV7	Select LV7 current magnitude to PA.
1	0	0	0	LV8	Select LV8 current magnitude to PB.
1	0	0	1	LV9	Select LV9 current magnitude to PB.
1	0	1	0	LV10	Select LV10 current magnitude to PB.
1	0	1	1	LV11	Select LV11 current magnitude to PB.
1	1	0	0	LV12	Select LV12 current magnitude to PB.
1	1	0	1	LV13	Select LV13 current magnitude to PB.
1	1	1	0	LV14	Select LV14 current magnitude to PB.
1	1	1	1	LV15	Select LV15 current magnitude to PB.

Note:

Turning on PA & PB simultaneously can cause over-current and permanent damage to the IC, high voltage MOSFETs, or to the transformer.

# **Board Connector and Test Pin Description**

CPLD Pin #	Signal Name	Description	
U2, 3 - 15, 26, 35	VCC	CPLD logic power supply +3.3V	
U2, 3 - 26	VLL	CPLD, VCCIO and MD2134 logic power supply +2.5V	
U2, 3 - 4, 17, 25	GND	Logic power ground 0V	
U2 - 2	WAV	Run or stop demo waveform phase	
U2 - 3	FRE	Selecting frequency: 8,10 and 13.3MHz	
U2 - 5	PHASE	Single step phase change, angle stepping:0, 7.5, 15360	
U2 - 6	AMPL	Single step amplitude change, DAC stepping: 15, 31255	
U2 - 7	ENA	Control MD2134 EN pin	
U2 - 18	M1	Output signal to MD2134 M1	
U2 - 19	MO	Output signal to MD2134 M0	
U2 - 20	M3	Output signal to MD2134 M3	
U2 - 21	M2	Output signal to MD2134 M2	
U3 - 31	LED1	Output signal yellow, PH0 LED is on when phase = 0	
U3 - 30	LED2	Output signal yellow, DAC LED is on when DAC = 127	
U3 - 27	PWR	Output signal LED green, indicates +3.3V power supply on	
U2, 3 - 10	TMS	Test mode select of JTAG	

# **Board Connector and Test Pin Description (cont.)**

CPLD Pin #	Signal Name	Description
U2, 3 - 9	TDI	Test data in of JTAG, two CPLD in daisy chain
U2, 3 - 24	TDO	Test data out of JTAG, two CPLD in daisy chain
U2, 3 - 11	TCK	Test clock of JTAG
U2, 3 - 43	CLK	CPLD clock input
U2, 3 - 39	EXTRG	External trigger signal input to control waveform timing
U2, 3 - 12	EN	Output signal LED red, indicates MD2134 is enabled
U3 - 22	SDI	Output signal to MD2134 SDI
U3 - 16	SDO	Input signal from MD2134 SDO
U3 - 23	SCK	Output signal to MD2134 SCK
U3 - 14	CS	Output signal to MD2134 CS
U3 - 13	LD	Output signal to MD2134 LD
All remaining pins		NC or Reserved

JTAG Connector Pin #	Signal Name	Description
J6-1	TMS	Test Mode Select of CPLD.
J6-2	TDI	Test Data In of CPLD.
J6-3	TDO	Test Data Out of CPLD.
J6-4	TCK	Test Clock of CPLD.
J6-5	GND	Logic power supply ground 0V for programming only.
J6-6	VCC	Logic power supply +3.3V for programming only.

Signal and Jumper Pin #	Signal Name	Description
J1	EXCLK	External clock input when on-board oscillator is disabled, or output of the clock when it is enabled.
J2	OSC_EN	Jumper for on-board oscillator, short = disabled, open = enabled.
J3	EXTRG	External trigger signal input.
J4	Load JP	Jumper for on-board RC load to MD2134DB2 high voltage output and XDCR connector.
J5	XDCR	MD2134DB2 waveform output, for SMA-cable to oscilloscope, <i>high voltage</i> ! 0 to +/-350V <sub>p-p</sub> max.

# **Power Supply Connector**

J7-1	VCC	+3.3V, MOSFET gate biasing and CPLD supply voltage with current limit from 120 to 150mA.	
J7-2	GND	Ground reference, 0V.	
J7-3	VDD	+5.0V MD2134 positive supply voltages with current limit to 50mA	
J7-4	GND	Ground reference, 0V.	
J7-5	VPP	+70 to100V, the high voltage supply with current limit to 30mA.	

### **Voltage Supply Power-Up Sequence**

Step	Signal Name	Description		
1	V <sub>DD</sub>	+5.0, MD2134 positive supply voltages		
2	V <sub>cc</sub>	+3.3V, MOSFET gate biasing and CPLD control logic supply voltage		
3	V <sub>PP</sub>	+70V to 100V, the high voltage supply		
4	EN Logic Active	Enable logic control, active-high signal to MD2134		

### **Voltage Supply Power-Down Sequence**

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1	EN Logic Active	Disable logic control, active-high signal to MD2134	
2	V <sub>PP</sub>	+70V to 100V, the high voltage supply, off	
3	V <sub>DD</sub>	+5.0V, MD2134 positive supply voltages with all input signals LOW, off	
4	V <sub>cc</sub>	+3.3, CPLD control logic supply voltage with EN = 0, off	

#### MD2134DB2 Bill of Materials

Reference	Description	Manufacturer's Part Number	Manufacturer
C1 - C12	Capacitor, 0.1µF, 25V, ceramic, X7R, 0603	NA	Any
C13, C14, C15	Capacitor, 0.027µF 50V ceramic, X7R 0603	ECJ-1VB1H273K	Panasonic
C18, C36	Capacitor, ceramic, 1.0µF 100V X7R 20% 1210	C3225X7R2A105M	TDK
C19	Capacitor, ceramic, 220pF 200V NP0 0805	ECJ-2YC2D221J	Panasonic
C32, C33, C34	Capacitor, 10µF 16V ELECT WT SMD	UWT1C100MCL1GB	Nichicon
C5, C28	Capacitor, ceramic, 3300pF, 10%, 100V, X7R, 0603	06031C332KAT2A	AVX
D1 - D4	LED: red, green, yellow, diff, 0805, SMD	NA	Any
D9	Diode Schottky, 100V, 1.0A, SMA	B1100-13	Diodes Inc.
D5 - D8	Diode Schottky, dual, 30V, SOT-363	BAT54DW-7	Diodes Inc.
L1	6.8µH coupled inductor (6x6x3.5mm)	LPD6235-682MGB	Coil Craft
L2	Short	NA	NA
R1-4	RES, 1/16W, 1%, 0603, SMD	NA	Any
R8, 9, 12, 15	RES, 1W, 1%, 2512, SMD	NA	Any
U1	IC ultrasound beamforming source driver 5x5mm 40-Lead QFN package	MD2134K7-G	Supertex Inc.
U2, U3	IC CPLD, 72 MCELL, C-Temp, 44-VQFP	XC9572XL-5VQ44C	Xilinx
U4	IC precision reference micropower ref, SOT-23	LM4040DEM3-2.5	National
U5	IC voltage regulator, 1.5A, 2.5V, SOT-223	ADP3339AKC-2.5	ADI
X1	Oscillator clock, 160.000MHZ, 3.3V, SMD	JITO-2-DC3AE-160	FOX Electronics

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