# **High Speed Ultrasound Beamforming Source Driver**

#### **Features**

- ► High resolution transmitting waveform
- ▶ Up to 3.0A push-pull source-driving current
- ► 230V<sub>P.P</sub> maximum output, uses two DN2625 FETs
- ► Angle vector beamforming I-Q switcher matrix
- ▶ 8-bit apodization DAC and 7.5° angular resolution
- ► Flexible frequency-resolution trade-off
- Programmable aperture windowing
- ▶ 250MHz maximum sampling rate
- 25MHz ultrasound maximum frequency
- ▶ PWM modulation push-pull current source
- Focusing phase adjustment & chirp waveform
- ▶ Fast SPI interface
- ▶ 2.5V CMOS logic interface
- ▶ +5.0V single power supply
- Low second order harmonic distortions

#### **Applications**

- Medical ultrasound imaging transmit beamforming
- High resolution NDT and Sonar phase arrays
- HIFU transducer phase arrays beamforming and focus scanning
- Piezoelectric & MEMS transducer waveform drivers
- High speed, high voltage, arbitrary waveform generator

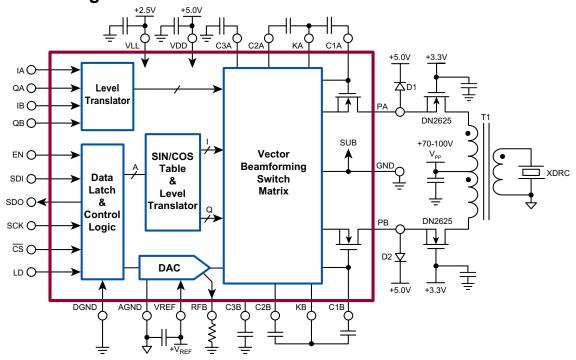
#### **General Description**

The MD2131 is a high-speed, arbitrary waveform, push-pull source driver. It is designed for medical ultrasound imaging and HIFU beamforming applications. It also can be used in NDT, Sonar and other ultrasound phase-array focusing beamforming applications.

The MD2131 consists of CMOS digital logic input circuits, an 8-bit current DAC for waveform amplitude control, and four PWM current-sources. These current sources are constructed with the high-speed, in-phase and quadrature current-switch matrix and the built-in sine and cosine angle-to-vector look-up table. The angular resolution of the vector table is 7.5° per step, with a total range of 48 steps. There are four logic input signals to control the in-phase and quadrature PWM push-pull current-source's output timing, frequency, cycle in the burst and waveform envelope.

The MD2131's output stage is designed to drive two DN2625 depletion N-type MOSFETs. The MOSFET drains are connected to a center-tap ultrasound frequency pulse transformer. The secondary winding of the transformer can connect to the ultrasound piezo or capacitive transducer via a cable with a good impendence match. The MD2131 has a high-speed, SPI-compatible interface to achieve per-scan-line fast updating of the data register for changing the beamforming phase angles and apodization amplitudes.

## MD2131 Block Diagram



#### **Ordering Information**

Device	40-Lead QFN 5.00x5.00mm body 0.80mm height (max) 0.40mm pitch
MD2131	MD2131K7-G

<sup>-</sup>G indicates package is RoHS compliant ('Green')

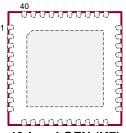
### **Absolute Maximum Ratings**

	<u> </u>
Parameter	Value
V <sub>LL</sub> , Logic supply	-0.5V to +3.5V
V <sub>DD</sub> , Positive supply	-0.5V to +6.0V
V <sub>PA</sub> V <sub>PB</sub> Driver outputs	-0.5V to +6.0V
V <sub>SUB</sub> , Ground	0V
Operating temperature	0°C to +70°C
Storage temperature	-65°C to +150°C
θ <sub>ja</sub> , Package thermal resistance (4"x3", 4-layer, 1oz, 16-via, PCB)	19°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

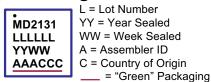


## **Pin Configuration**



40-Lead QFN (K7) (top view)

## **Package Marking**



Package may or may not include the following marks: Si or 🏟

40-Lead QFN (K7)

#### **Operating Supply Voltages**

(Over operating conditions unless otherwise specified,  $V_{LL}$  = +2.5V,  $V_{DD}$  = +5.0V,  $R_{FB}$  = 50k $\Omega$ , DAC = 0,  $V_{REF}$  = 2.5V,  $T_{A}$  = 25°C)

Sym	Parameter	Min	Тур	Max	Units	Conditions
V <sub>LL</sub>	Logic supply	2.3	2.5	2.7	V	T = 0 to 70°C
V <sub>DD</sub>	Power supply	4.75	5.00	5.25	V	$T_A = 0 \text{ to } 70^{\circ}\text{C}$
I <sub>LLQ</sub>	V <sub>LL</sub> supply current EN = 0	-	0.1	1.0		Standby condition
I <sub>DDQ</sub>	V <sub>DD</sub> supply current EN = 0	-	0.2	1.0	μA	Standby condition
ILLEN	V <sub>LL</sub> supply current EN = 1	-	5.0	20	μA	f = 0 all logic input no transit
I <sub>DDEN</sub>	V <sub>DD</sub> supply current EN = 1	-	5.0	12	mA	f <sub>CLK</sub> = 0, all logic input no transit
I <sub>LL50</sub>	V <sub>LL</sub> supply current EN = 1	-	0.5	3.0	mA	f <sub>CLK</sub> = 50MHz, CW, IA, IB, QA, QB = 0
I <sub>DD50</sub>	V <sub>DD</sub> supply current EN = 1	-	80	-	mA	EN = 1, IA, IB, QA, QB = 50MHz, CW

Output Characteristics (Over operating conditions unless otherwise specified,  $V_{LL}$  = +2.5V,  $V_{DD}$  = +5.0V,  $V_{REF}$  = 2.5V,  $R_{FB}$  = 50k $\Omega$ , Angle = 45° IA = QA = Hi or IB = QB = Hi of 1 $\mu$ s, D% = 0.1%,  $T_A$  = 25°C)

Sym	Parameter	Min	Тур	Max	Units	Conditions
I <sub>MAX-A/B</sub>	Full scale output peak current	2.7	-	3.3	Α	DAC = 255
I <sub>OO-A/B</sub>	Output current offset	-	0.5	1.0	mA	DAC = 0
	Output voltage range, +10% of I <sub>PA/B</sub>	5.3	5.8	-		I <sub>PA/B</sub> = 1.0A
		5.0	5.5	-		I <sub>PA/B</sub> = 1.5A
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	PA/B	4.5	5.0	-		I <sub>PA/B</sub> = 3.0A
$V_{PA}, V_{PB}$		-	1.0	1.5		I <sub>PA/B</sub> = 1.0A
	Output voltage range, -10% of I <sub>PA/B</sub>	-	1.2	1.7		I <sub>PA/B</sub> = 1.5A
		-	1.8	2.3		I <sub>PA/B</sub> = 3.0A

Aperture DAC Characteristics (Over operating conditions unless otherwise specified,  $V_{LL}$  = +3.3V,  $V_{DD}$  = +5V,  $R_{FB}$  = 50k $\Omega$ ,  $T_A$  = 25°C)

Sym	Parameter	Min	Тур	Max	Units	Conditions
Reso	Resolution	-	8	_	Bits	
E <sub>LINEAR</sub>	Linearity error	-	1.0	3.0	%	±% of FSR
E <sub>DNL</sub>	Differential nonlinearity error	-	0.6	1.0	%	±% of FSR
MON	Monotonicity	-	8	-	Bits	
V <sub>REF</sub>	External reference voltage	1.25	-	2.5	V	

**Logic and Data Input Characteristics** (Over operating conditions unless otherwise specified,  $V_{LL}$  = +3.3V,  $V_{DD}$  = +5V,  $R_{FB}$  = 50k $\Omega$ ,  $T_A$  = 0 - 70°C)

Sym	Parameter	Min	Тур	Max	Units	Conditions
V <sub>IH</sub>	Input logic high voltage	0.8V <sub>LL</sub>	-	V <sub>LL</sub>	V	
V <sub>IL</sub>	Input logic low voltage	0	-	0.2V <sub>LL</sub>	V	
I <sub>IH</sub>	Input logic high current	-	-	1.0	μA	
I <sub>IL</sub>	Input logic low current	-1.0	-	-	μA	

#### **AC Electrical Characteristics**

(Over operating conditions unless otherwise specified,  $V_{v,z} = +3.3V$ ,  $V_{v,z} = +5V$ ,  $R_{v,z} = 50k\Omega$ ,  $T_{v,z} = 25^{\circ}C$ )

Sym	Parameter	Min	Тур	Мах	Units	
t <sub>st</sub>	DAC to output setup time	-	-	10	μs	All caps 10nF, DAC = 0 to 255, settle to 1LSB
t <sub>r</sub>	Output current rise time	-	2.0	3.0		1.0Ω resistor load to $V_{DD}$ ,
t <sub>f</sub>	Output current fall time	_	2.0	3.0	ns	DAC = 85,
t <sub>dr</sub>	Input to output delay on rise	-	4.0	5.0	115	Angle = 45°,
t <sub>df</sub>	Input to output delay on fall	-	4.0	5.0		V <sub>REF</sub> = 2.5V
t <sub>M</sub>	Delay time matching	-	±2.0	±3.0	ns	From PA to PB and device to device
t <sub>J</sub>	Output jitter	-	50	-	ps	
t <sub>1</sub>	SDI valid to SCK setup time	0	2.0	-		Con agriculintorfore timing diagrams
t <sub>2</sub>	SDI valid to SCK hold time	4.0	-	-	ns	See serial interface timing diagram
t <sub>3</sub>	SCK high time (% of 1/f <sub>SCK</sub> )	45	_	55	%	Con agriculintorfore timing diagrams
t <sub>4</sub>	SCK low time (% of 1/f <sub>SCK</sub> )	45	_	55	%	See serial interface timing diagram
t <sub>5</sub>	CS pulse width	4.0	-	6.0		
t <sub>6</sub>	LSB SCK high to CS high	7.0	-	ı		
t <sub>7</sub>	CS low to SCK high	7.0	-	-		
t <sub>8</sub>	SDO propagation delay from SCK failing edge	-	-	10	ns	See serial interface timing diagram
t <sub>9</sub>	CS high to SCK raising edge	7.0	-	-		
t <sub>10</sub>	CS high to LD raising edge	10	-	-		
f <sub>sck</sub>	Serial clock maximum frequency	40	50	-	MHz	
THD	Total harmonic distortion	-	-45	-40	dB	
t <sub>EN-OFF</sub>	EN fall to PA/PB turn OFF time	_	5.0	8.0	ns	50% to 90%
t <sub>EN-ON</sub>	EN rise to PA/PB turn ON time	-	13.5	20.0	μs	50% to 10%

#### **Serial Register Description**

Comi	mand	MSB	MSB DAC Value Register					LSB	MSB	Vec	tor Ang	le Regi	ster	LSB	
C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0

#### **Command Description**

Con	nmand	Description				
C1	C0	Description				
0	0	Write to input register				
0	1	Read register				
1	0	Power down triggered at C[1:0] = 10 and cs rise edge, other state power-up				
1	1	No operation				

#### **DAC Input and Output Description**

MSB			DAC Valu	e Register	•		LSB	PA/PB Output Current		
D7	D6	D5	D4	D3	D2	D1	D0	FAIFB Output Guilent		
0	0	0	0	0	0	0	0	(0/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		
0	0	0	0	0	0	0	1	(1/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		
0	1	1	1	1	1	1	1	(127/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		
1	0	0	0	0	0	0	0	(128/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		
1	1	1	1	1	1	1	0	(254/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		
1	1	1	1	1	1	1	1	(255/255)I <sub>MAX-A/B</sub> + I <sub>OO-A/B</sub>		

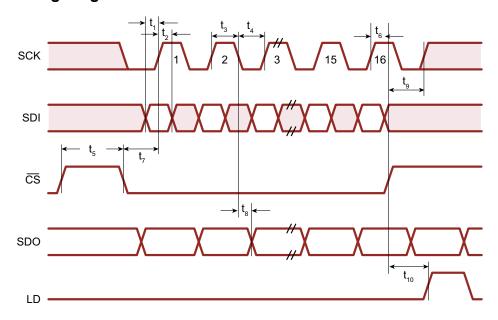
## Angle Register and I/Q Vector Description

MSB		Angle F	Register		LSB	Angle	I-Vector (6-bit)	Q-Vector (6-bit)
<b>A5</b>	A4	А3	A2	<b>A1</b>	A0	Degree	cos	SIN
0	0	0	0	0	0	0	111111	000000
0	0	0	0	0	1	7.5	111110	001000
0	0	0	1	1	0	45¹	101101	101101
0	0	1	1	0	0	90	000000	111111
0	1	0	0	1	0	135	-101101	101101
0	1	1	0	0	0	180	-111111	000000
0	1	1	1	1	0	225	-101101	-101101
1	0	0	1	0	0	270	-000000	-111111
1	0	1	0	1	0	315	101101	-101101
1	0	1	1	1	1	352.5	111110	-001000
1	1	0	0	0	0	360 = 0 <sup>2</sup>	111111	000000

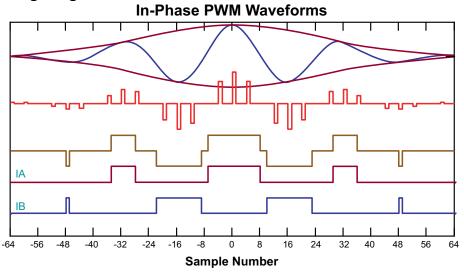
#### Notes:

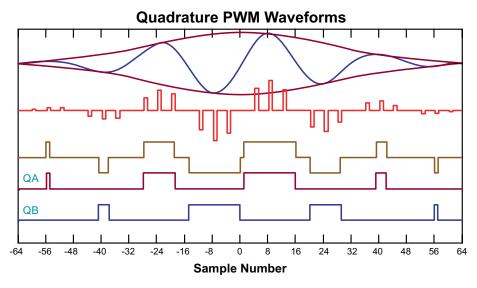
- 1. Maximum current magnitude of output PA or PB is at 45° angle, when IA = QA = Hi or IB = QB = Hi.
- Angle>110000B (48) are reserved states.

## **Serial Interface Timing Diagram**



#### **PWM Interface Timing Diagram**





#### In-Phase and Quadrature Output Current Equations

The in-phase and quadrature phase output sinking current magnitudes,  $\rm I_i$  and  $\rm I_q$ , can be calculated by the following equations:

$$I_{i} = \frac{24 \cdot V_{REF} \cdot DAC \cdot (2^{6} - 1) \cdot cos(\alpha)}{9 \cdot R_{FB}}$$

$$I_{q} = \frac{24 \cdot V_{REF} \cdot DAC \cdot (2^{6} - 1) \cdot sin(\alpha)}{9 \cdot R_{FB}}$$

Where the  $V_{REF}$  is the voltage reference, DAC is the decimal value of the data in the DAC register,  $R_{FB}$  is the setting resistor value in ohms, and  $\alpha$  is the value of the vector angle in degrees.

The absolute values of the results from the equations represent the magnitude of the output sinking current. The plus or minus sign of the results indicate the current flow in to the output port PA or PB, respectively. Note that the maximum full scale of pulse current at PA or PB port only can be obtained at DAC = 255,  $V_{REF}$  = 2.5V,  $R_{FB}$  = 50k $\Omega$ ,  $\alpha$  = 45° and IA = QA = Hi or IB = QB = Hi conditions.

## **Pin Description**

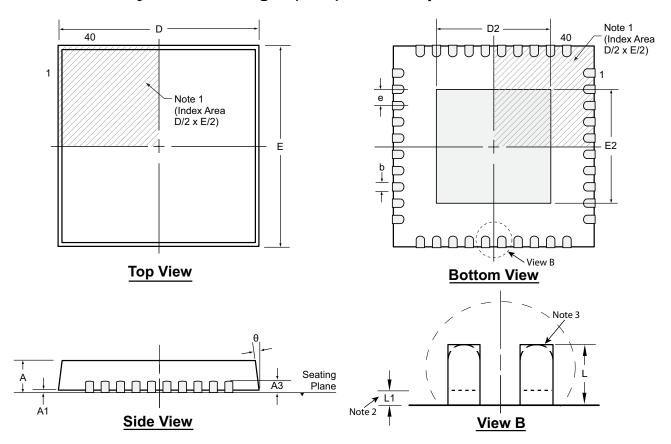
Pin #     Function     Description       1     KA     Kelvin connection A       2     GND     High current output ground       3     C1A     Bypass cap KA, 10nF low ESR X7R ceramic cap	
2 GND High current output ground 3 C1A Bypass cap KA, 10nF low ESR X7R ceramic cap	
3 C1A Bypass cap KA, 10nF low ESR X7R ceramic cap	
4 GND High current output ground	
5 VDD Supplies voltage of the gate driver and internal analog circuit	
6 C3A Bypass cap to GND of Pin#7, 10nF low ESR X7R ceramic cap	
7 GND High current output ground	
8 VLL Supply voltage of logic circuit	
9 DGND Digital logic ground	
10 SCK Serial clock input	
The state of the s	
14 IA PWM control logic input of in-phase A	
15 IB PWM control logic input of in-phase B	
16 VDD Supplies voltage of the gate driver and internal analog circuit	
17 AGND Analog reference ground	
18 SDO Serial data output, updated at SCK falling edge	
19 CS Serial chip select, active low, and buffer register loading clock on rising edge	
20 LD DAC data register loading clock on rising edge	
21 EN Enable, EN = Low, PA = PB = Hi-Z	
22 VREF External reference voltage input	
23 RFB Resistor to GND, 50kΩ 0.1% for the best accuracy	
24 GND High current output ground	
25 C3B Bypass cap to GND of Pin#24, 10nF low ESR X7R ceramic cap	
26 VDD Supplies voltage of the gate driver and internal analog circuit	
27 GND High current output ground	
28 C1B Bypass cap to KB, 10nF low ESR X7R ceramic cap	
29 GND High current output ground	
30 KB Kelvin connection B	
31 C2B Bypass cap to KB, 10nF low ESR X7R ceramic cap	
32 PB Current sinking source driver output B, external Schottky diode to VDD	
33 PB Current sinking source driver output B, external Schottky diode to VDD	
34 PB Current sinking source driver output B, external Schottky diode to VDD	
35  VSUB  Substrate voltage must connected to the lowest potential of the IC, the ground	
36 Substrate voltage must connected to the lowest potential of the 10, the ground	
37 PA Current sinking source driver output A, external Schottky diode to VDD	
38 PA Current sinking source driver output A, external Schottky diode to VDD	
39 PA Current sinking source driver output A, external Schottky diode to VDD	
40 C2A Bypass Cap to KA, 10nF low ESR X7R ceramic cap	

#### Notes:

- Pins #35 & #36 are VSUB connected to the center thermal pad internally in the package.
   All bypass capacitors need be very close to the pins

# 40-Lead QFN Package Outline (K7)

### 5.00x5.00mm body, 0.80mm height (max), 0.40mm pitch



#### Notes:

- 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- 2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
- 3. The inner tip of the lead may be either rounded or square.

Symbol		Α	A1	А3	b	D	D2	E	E2	е	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.15	4.85*	3.45	4.85*	3.45	0.40 BSC	0.25 <sup>†</sup>	0.00	0°
	NOM	0.75	0.02		0.20	5.00	3.60	5.00	3.60		0.35 <sup>†</sup>	-	-
	MAX	0.80	0.05		0.25	5.15*	3.70 <sup>†</sup>	5.15*	3.70 <sup>†</sup>		0.45 <sup>†</sup>	0.15	14º

JEDEC Registration MO-220, Variation WHHE-1, Issue K, June 2006

Drawings not to scale.

Supertex Doc. #: DSPD-40QFNK75X5P040, Version C041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="http://www.supertex.com/packaging.html">http://www.supertex.com/packaging.html</a>.)

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<sup>\*</sup> This dimension is not specified in the JEDEC drawing.

<sup>†</sup> This dimension differs from the JEDEC drawing.