High Speed Ultrasound Beamforming Source Driver

Features

- High resolution transmitting waveform
- Up to 3.0A push-pull source-driving current
- 160MHz maximum, 3ns time resolution
- 250V_{P-P} maximum output, use two DN2625 MOSFETs
- Angle vector beamforming I-Q switcher matrix
- 8-bit apodization DAC and 7.5° angular resolution
- Flexible frequency-resolution trade-off
- Programmable aperture windowing
- PWM modulation push-pull current source
- Focusing phase adjustment & chirp waveform
- Per-scan-line updating with SPI compatible interface
- 1.8 to 3.3V CMOS logic interface
- +5.0V single power supply
- Low second order harmonic distortions

Applications

- Medical imaging ultrasound beamforming transmitter
- High resolution NDT and Sonar phase array driver
- Ultrasonic phase array focusing transmitter
- Piezoelectric & MEMS transducer waveform drivers
- High speed arbitrary waveform generator

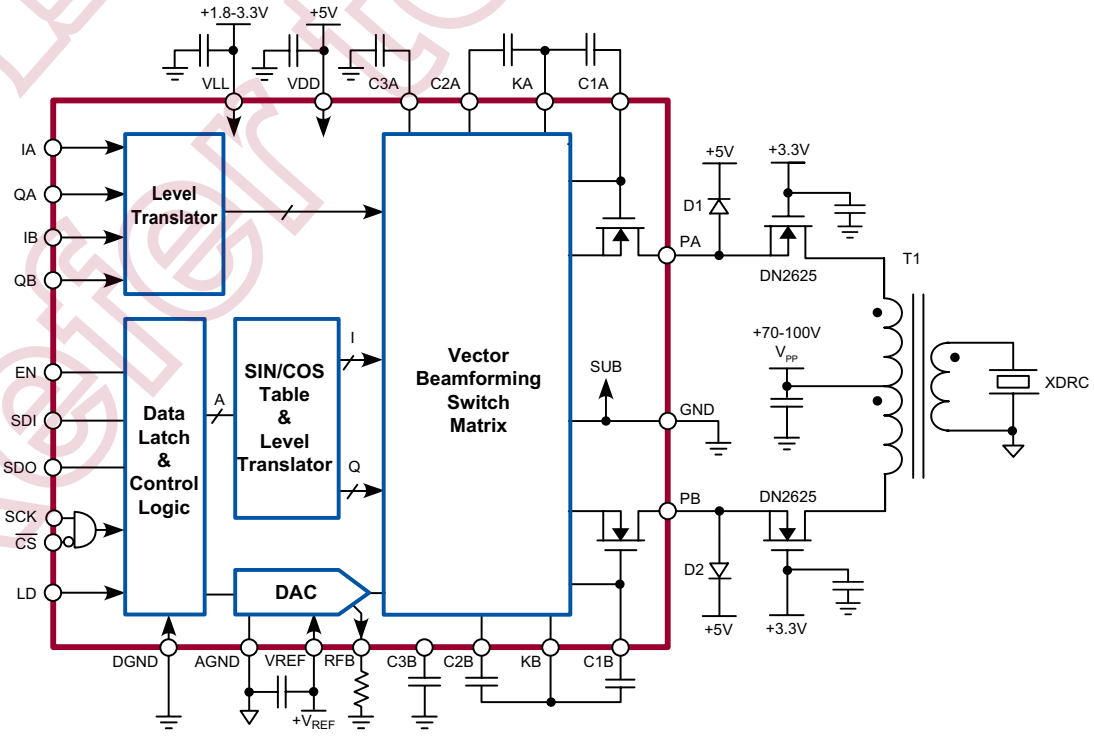
General Description

MD2130 is a high-speed arbitrary waveform push-pull source-driver. It is designed for medical ultrasound imaging and HIFU beamforming applications.

The IC consists of CMOS digital logic input circuits, an 8-bit current DAC for the waveform amplitude control and four PWM current-sources. These current sources are constructed with a high-speed in-phase and quadrature current-switch matrix and the built-in sine and cosine angle-to-vector look-up table. The angular resolution of the vector table is 7.5° per step with total range of 48 steps. There are four logic input signals to control the in-phase and quadrature PWM push-pull current-source's output timing, frequency, cycle in the burst and waveform envelope.

MD2130's output stage is designed to drive two depletion mode high-voltage DN2625 N-type MOSFETs as the source-driver. The MOSFET drains are connected to a center-tap ultrasound frequency pulse transformer. The secondary winding of the transformer can connect to the ultrasound piezo or capacitive transducer via cable and with a good impendence match. MD2130 has the high-speed SPI compatible interface to achieve per-scan-line fast updating the data register for changing the beamforming phase angles and apodization amplitudes.

Block Diagram



Ordering Information

Device	40-Lead QFN *5.00x5.00mm body* *0.80mm height (max)* *0.40mm pitch*
MD2130	MD2130K7-G

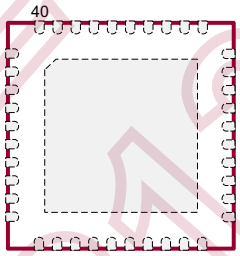
*-G indicates package is RoHS compliant ('Green') * Au plating*

Absolute Maximum Ratings

Parameter	Value
V_{LL}, Logic supply	-0.5V to +5.0V
V_{DD}, Positive supply	-0.5V to +6V
V_{PA} V_{PB} Driver outputs	-0.5V to +6V
V_{SUB}, Ground	0V
Operating temperature	0°C to +70°C
Storage temperature	-55°C to +150°C
θ_{ja}, Package thermal resistance *(4"x3", 4-layer 1oz 16-via PCB)*	19°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



40-Lead QFN (K7)
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

Package may or may not include the following marks: Si or ⏻

40-Lead QFN (K7)

Operating Supply Voltages

(Over operating conditions unless otherwise specified, V_{LL} = +3.3V, V_{DD} = +5V, R_{FB} = 50kΩ, DAC = 0, V_{REF} = 2.5V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic supply	1.8	3.3	3.6	V	T_A = 0 to 70°C
V_{DD}	Power supply	4.75	5.0	5.25	V	
I_{LLQ}	V_{LL} supply current EN = 0	-	0.1	0.2	µA	Standby condition
I_{DDQ}	V_{DD} supply current EN = 0	-	0.2	1.0		
I_{LLEN}	V_{LL} supply current EN = 1	-	5.0	50	µA	f_{CLK} = 0, all logic input no transit
I_{DDEN}	V_{DD} supply current EN = 1	-	5.0	12	mA	
I_{LL50}	V_{LL} supply current EN = 1	-	0.5	3.0	mA	f_{CLK} = 50MHz, CW, IA, IB, QA, QB = 0
I_{DD50}	V_{DD} supply current EN = 1	-	25	65	mA	EN = 1, IA, IB, QA, QB = 50MHz, CW

Output Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +3.3V, V_{DD} = +5V, V_{REF} = 2.5V, R_{FB} = 50kΩ, Angle = 45° IA = QA = Hi or IB = QB = Hi of 1µs, D% = 0.1%, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{MAX-A/B}$	Full scale output peak current	2.7	-	3.3	A	*DAC = 255*
$I_{OO-A/B}$	Output current offset	-	0.5	2.0	mA	*DAC = 0*
V_{PA}, V_{PB}	Output voltage range, +10% of $I_{PA/B}$	5.3	5.8	-	V	$I_{PA/B}$ = 1.0A
		5.0	5.5	-		$I_{PA/B}$ = 1.5A
		4.5	5.0	-		$I_{PA/B}$ = 3.0A
	Output voltage range, -10% of $I_{PA/B}$	-	1.0	1.5		$I_{PA/B}$ = 1.0A
		-	1.2	1.7		$I_{PA/B}$ = 1.5A
		-	1.8	2.3		$I_{PA/B}$ = 3.0A

Aperature DAC Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +3.3V, V_{DD} = +5V, R_{FB} = 50kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
Reso	Resolution	-	8	8	Bits	---
E_{LINEAR}	Linearity error	-	1.0	2.0	%	±% of FSR
E_{DIFF}	Differential nonlinearity	-	1.0	2.0	%	±% of FSR
MON	Monotonicity	-	8	8	Bits	---
V_{REF}	External reference voltage	1.25	-	2.5	V	---

Logic and Data Input Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +3.3V, V_{DD} = +5V, R_{FB} = 50kΩ, T_A = 0 - 70°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	$0.8V_{LL}$	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{LL}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---

AC Electrical Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +3.3V, V_{DD} = +5V, R_{FB} = 50kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{OUT}	Output frequency range	1.0	-	20	MHz	---
t_{ST}	DAC to output setup time	-	50	80	µs	All caps 27nF, settle to 1LSB
t_r	Output current rise time	-	3.0	10	ns	1.0Ω resistor load to V_{DD}, DAC = 85, Angle = 45°, V_{REF} = 2.5V
t_f	Output current fall time	-	3.0	10		
t_{dr}	Input to output delay on rise	2.6	-	5.6		
t_{df}	Input to output delay on fall	2.6	-	5.6		
t_M	Delay time matching	-	±2.0	±3.0	ns	From PA to PB and device to device
t_J	Output jitter	-	12	-	ps	PWM input to N-FET drain with 100Ω resistor load and +25V V_{PP}
t_1	SDI valid to SCK setup time	0	2.0	-	ns	See serial interface timing diagram
t_2	SDI valid to SCK hold time	4.0	-	-		
t_3	SCK high time	9.0	-	-		
t_4	SCK low time	9.0	-	-		
t_5	CS pulse width	9.0	-	-		
t_6	LSB SCK high to CS high	7.0	-	-		
t_7	CS low to SCK high	7.0	-	-		
t_8	SDO propagation delay from SCK failing edge	-	-	85		
t_9	CS high to SCK raising edge	7.0	-	-		
t_{10}	CS high to LD raising edge	10	-	-		
f_{SCK}	Serial clock maximum frequency	50	-	-	MHz	20MHz max. when V_{LL} = 1.8V
THD	Total harmonic distortion	-	-45	-40	dB	---

Serial Register Description

Command		MSB			DAC Value Register				LSB	MSB		Vector Angle Register			LSB
C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0

Command Description

Command		Description
C1	C0	
0	0	Write to input register
0	1	Read register
1	0	Power down
1	1	No operation

DAC Input and Output Description

MSB			DAC Value Register				LSB	PA/PB Output Current
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	$(0/255)I_{MAX-A/B} + I_{OO-A/B}$
0	0	0	0	0	0	0	1	$(1/255)I_{MAX-A/B} + I_{OO-A/B}$
0	1	1	1	1	1	1	1	$(127/255)I_{MAX-A/B} + I_{OO-A/B}$
1	0	0	0	0	0	0	0	$(128/255)I_{MAX-A/B} + I_{OO-A/B}$
1	1	1	1	1	1	1	0	$(254/255)I_{MAX-A/B} + I_{OO-A/B}$
1	1	1	1	1	1	1	1	$(255/255)I_{MAX-A/B} + I_{OO-A/B}$

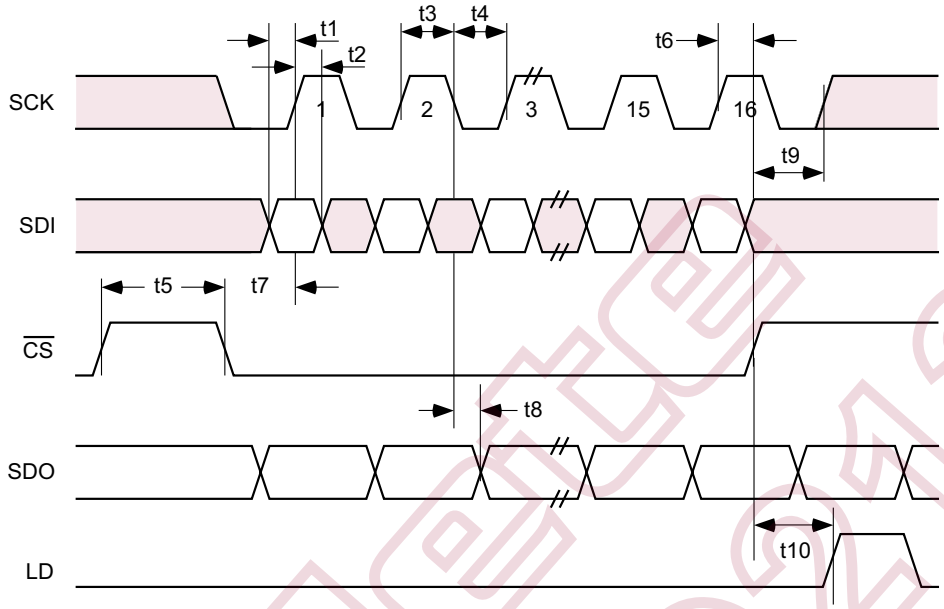
Angle Register and I/Q Vector Description

MSB			Angle Register		LSB	Angle	I-Vector (6-bit)	Q-Vector (6-bit)
A5	A4	A3	A2	A1	A0	Degree	COS	SIN
0	0	0	0	0	0	0	111111	000000
0	0	0	0	0	1	7.5	111110	001000
0	0	0	1	1	0	45 (1)	101101	101101
0	0	1	1	0	0	90	000000	111111
0	1	0	0	1	0	135	-101101	101101
0	1	1	0	0	0	180	-111111	000000
0	1	1	1	1	0	225	-101101	-101101
1	0	0	1	0	0	270	-000000	-111111
1	0	1	0	1	0	315	101101	-101101
1	0	1	1	1	1	352.5	111110	-001000
1	1	0	0	0	0	360 = 0 (2)	111111	000000

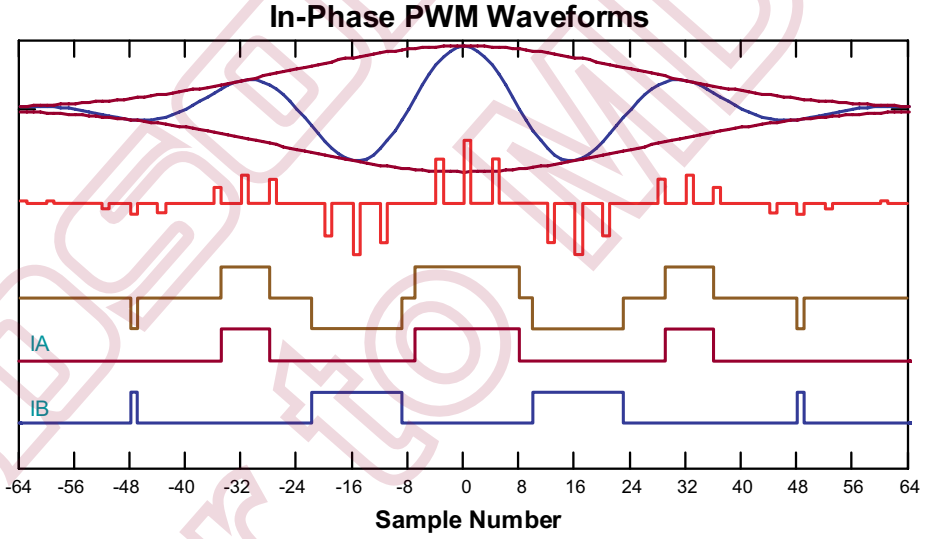
Notes:

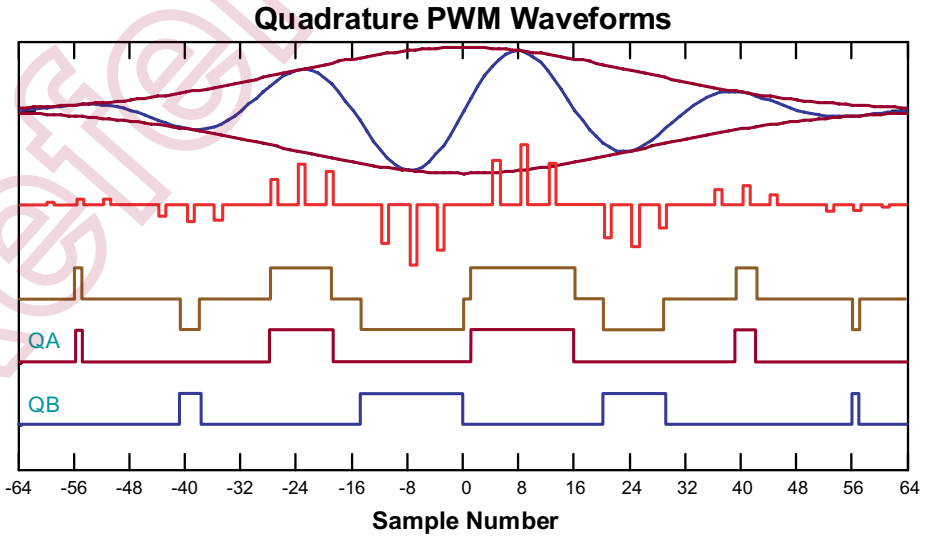
1. *Maximum current magnitude of output PA or PB is at 45° angle, when IA = QA = Hi or IB = QB = Hi.*
2. *Angle>110000B (48) are reserved states.*

Serial Interface Timing Diagram



PWM Interface Timing Diagram





PWM Input and Angle vs. Output Current Port

Phase angle (α)		cos (α) > 0	cos (α) < 0
PWM Input Hi at:	IA	PA	PB
	IB	PB	PA
		sin (α) > 0	**sin (α) < 0**
	QA	PA	PB
	QB	PB	PA

In-Phase and Quadrature Output Current Equations

The in-phase and quadrature phase output sinking current magnitudes, I_i and I_q, can be calculated by the following equations:

$$I_i = \frac{24 \cdot V_{REF} \cdot DAC \cdot (2^6 - 1) \cdot \cos(\alpha)}{9 \cdot R_{FB}}$$

$$I_q = \frac{24 \cdot V_{REF} \cdot DAC \cdot (2^6 - 1) \cdot \sin(\alpha)}{9 \cdot R_{FB}}$$

Where the V_{REF} is the voltage reference, DAC is the decimal value of the data in the DAC register, R_{FB} is the setting resistor value in ohms, α is the value of the vector angle in degree.

The absolute values of the results from the equations represent the magnitude of the output sinking current. The plus or minus sign of the results indicate the current flow in to the output port PA or PB, respectively. Note that the maximum full scale of pulse current at PA or PB port only can be obtained at DAC = 255, V_{REF} = 2.5V, R_{FB} = 50kΩ, α = 45° and IA = QA = Hi or IB = QB = Hi conditions.

Pin Description

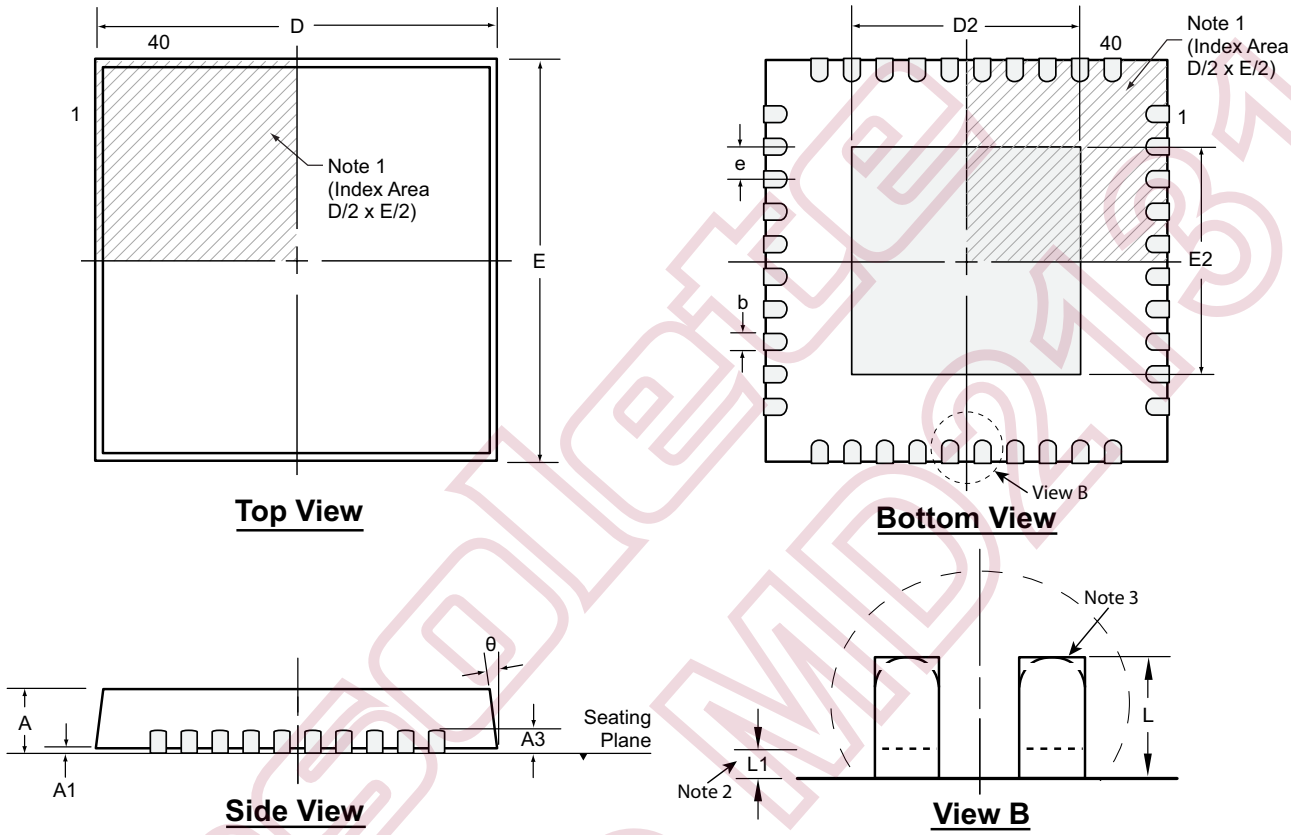
Pin #	Function	Description
1	KA	Kelvin connection A
2	GND	High current output ground
3	C1A	Bypass cap KA, 27nF low ESR X7R ceramic cap
4	GND	High current output ground
5	VDD	Supplies voltage of the gate driver and internal analog circuit
6	C3A	Bypass cap to GND of Pin#7, 27nF low ESR X7R ceramic cap
7	GND	High current output ground
8	VLL	Supply voltage of logic circuit
9	DGND	Digital logic ground
10	SCK	Serial clock input
11	SDI	Serial data input
12	QA	PWM control logic input of quadrature-phase A
13	QB	PWM control logic input of quadrature-phase B
14	IA	PWM control logic input of in-phase A
15	IB	PWM control logic input of in-phase B
16	VDD	Supplies voltage of the gate driver and internal analog circuit
17	AGND	Analog reference ground
18	SDO	Serial data output
19	CS	Serial chip select, active low, and buffer register loading clock on rising edge
20	LD	DAC data register loading clock on rising edge
21	EN	Enable, EN = Low, PA = PB = Hi-Z and all internal registers freeze until next clock rising edge
22	VREF	External reference voltage input
23	RFB	Resistor to GND, 50kΩ 0.1% for the best accuracy
24	GND	High current output ground
25	C3B	Bypass cap to GND of Pin#24, 27nF low ESR X7R ceramic cap
26	VDD	Supplies voltage of the gate driver and internal analog circuit
27	GND	High current output ground
28	C1B	Bypass cap to KB, 27nF low ESR X7R ceramic cap
29	GND	High current output ground
30	KB	Kelvin connection B
31	C2B	Bypass cap to KB, 27nF low ESR X7R ceramic cap
32	PB	Current sinking source driver output B, external Schottky diode to VDD
33	PB	Current sinking source driver output B, external Schottky diode to VDD
34	PB	Current sinking source driver output B, external Schottky diode to VDD
35	VSUB	Substrate voltage must connected to the lowest potential of the IC, the ground
36		
37	PA	Current sinking source driver output A, external Schottky diode to VDD
38	PA	Current sinking source driver output A, external Schottky diode to VDD
39	PA	Current sinking source driver output A, external Schottky diode to VDD
40	C2A	Bypass Cap to KA, 27nF low ESR X7R ceramic cap

Notes:

1. *Pin # 35 & #36 are VSUB connected to the center thermal pad internally in the package.*
2. *All bypass capacitors need be very close to the pins*

40-Lead QFN Package Outline (K7)

5.00x5.00mm body, 0.80mm height (max), 0.40mm pitch



Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.15	4.85*	3.45	4.85*	3.45	0.40 BSC	0.25†	0.00	0°
	NOM	0.75	0.02		0.20	5.00	3.60	5.00	3.60		0.35†	-	-
	MAX	0.80	0.05		0.25	5.15*	3.70†	5.15*	3.70†		0.45†	0.15	14°

JEDEC Registration MO-220, Variation WHHE-1, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-40QFNK75X5P040, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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