

## Low Harmonic Distortion, 32-Channel, High Voltage Analog Switch IC

### Features

- ▶ 32 Channels of high voltage analog switch
- ▶ 2:1 Multiplexer / Demultiplexer
- ▶ 3.3 or 5.0V CMOS input logic level
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation -10 $\mu$ A
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Flexible operating supply voltages

### Applications

- ▶ Electromechanical relay replacement in medical ultrasound probes.

### General Description

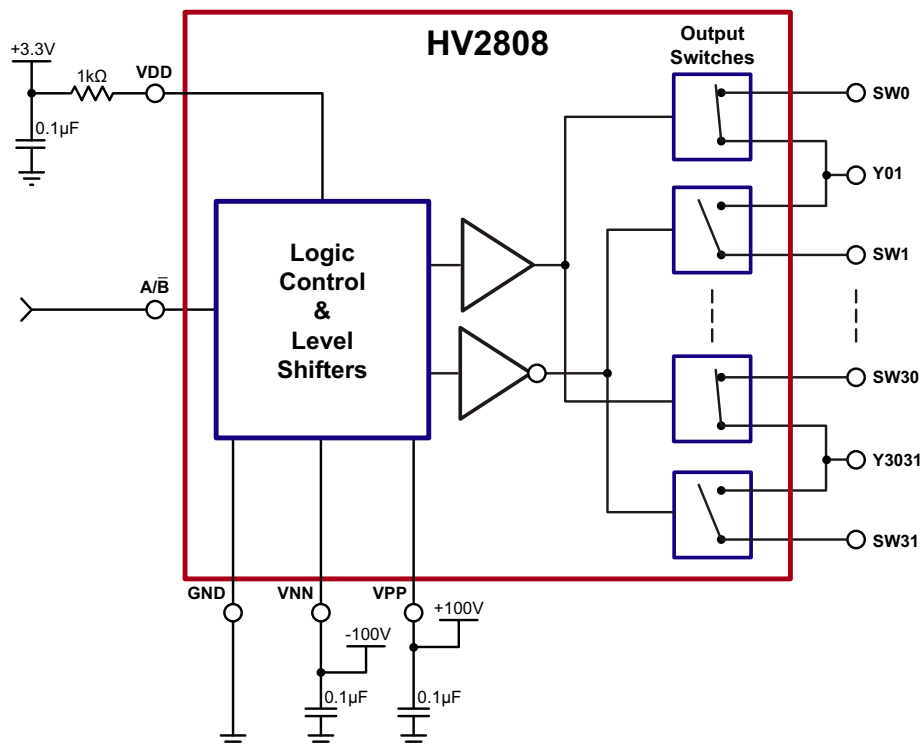
The Supertex HV2808 is a low harmonic distortion, 32-channel, high voltage analog switch integrated circuit (IC), designed for use in medical ultrasound imaging systems as a probe selection relay replacement. It serves as a 16PDT (16-pole, double throw) high voltage analog switch array. HV2808 is a very fast transducer multiplexer that consumes minimal power and emits no audible noise.

Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V, and +160V/-40V.

The HV2808 comes in an 8x8x1.0mm, 56-Lead QFN package. Compared to an electromechanical relay, it not only saves considerable PCB area, but also saves on the PCB assembled height.

### Block Diagram



## Ordering Information

Part Number	Package Option	Packing
HV2808K6-G	56-Lead QFN (8x8)	250/Tray
HV2808K6-G M937	56-Lead QFN (8x8)	2000/Reel

-G indicates package is RoHS compliant ("Green")



## Absolute Maximum Ratings

Parameter	Value
$V_{DD}$ logic supply	-0.5V to +6.5V
$V_{PP}$ - $V_{NN}$ differential supply	220V
$V_{PP}$ positive supply	-0.5V to $V_{NN}$ +200V
$V_{NN}$ negative supply	+0.5V to -200V
Logic input voltage	-0.5V to $V_{DD}$ +0.3V
Analog signal range	$V_{NN}$ to $V_{PP}$
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Thermal resistance, $\theta_{ja}$	27°C/W
Thermal resistance, $\theta_{jc}$	0.5°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Typical Thermal Characteristics

Package	$\theta_{ja}$
56-Lead QFN (K6)	21°C/W

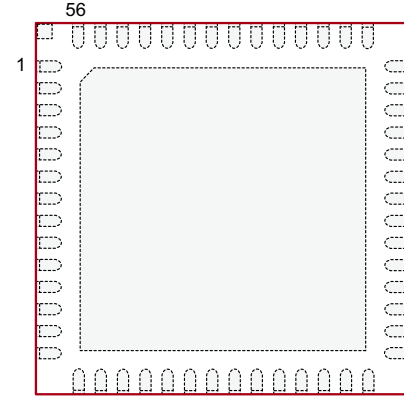
## Recommended Operating Conditions

Sym	Parameter	Value
$V_{DD}$	Logic power supply voltage	3.0 to 5.5V
$V_{PP}$	Positive high voltage supply	+40 to $V_{NN}$ +200V
$V_{NN}$	Negative high voltage supply	-40 to -160V
$V_{IH}$	High level input voltage	0.9 $V_{DD}$ to $V_{DD}$
$V_{IL}$	Low level input voltage	0 to 0.1 $V_{DD}$
$V_{SIG}$	Analog signal voltage peak-to-peak	$V_{NN}$ +10V to $V_{PP}$ -10V
$T_A$	Operating free air temperature	0 to 70°C

**Notes:**

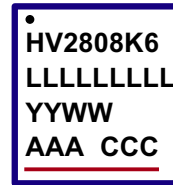
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2.  $V_{SIG}$  must be  $V_{NN} \leq V_{SIG} \leq V_{PP}$  or floating during power up/down transition.
3. Rise and fall times of power supplies  $V_{DD}$ ,  $V_{PP}$  and  $V_{NN}$  should not be less than 1.0msec.

## Pin Configuration



56-Lead QFN (K6)  
(top view)

## Product Marking



L = Lot Number  
 YY = Year Sealed  
 WW = Week Sealed  
 A = Assembler ID  
 C = Country of Origin  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

56-Lead QFN (K6)

**DC Electrical Characteristics** (Over recommended operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
R <sub>ONS</sub>	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	25	-	22	27	-	32		I <sub>SIG</sub> = 200mA
		-	25	-	22	27	-	30		I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	18	-	18	24	-	27		I <sub>SIG</sub> = 200mA
		-	23	-	20	25	-	30		I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V
		-	22	-	16	25	-	27		I <sub>SIG</sub> = 200mA
ΔR <sub>ONS</sub>	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
R <sub>ONL</sub>	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 1A
I <sub>SOL</sub>	Switch OFF-leakage per switch	-	5.0	-	1.0	1.0	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V, V <sub>NN</sub> +10V
V <sub>OS</sub>	DC offset switch OFF	-	300	-	100	300	-	300	mV	No load
	DC offset switch ON	-	500	-	100	500	-	500		
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches OFF
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-		
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches ON, I <sub>SW</sub> = 5.0mA
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-		
I <sub>SW</sub>	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V <sub>SIG</sub> duty cycle < 0.1%
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%
I <sub>PP</sub>	Average V <sub>PP</sub> supply current	-	13	-	-	14	-	16	mA	All output switches are turning ON and OFF at 50kHz with no load
		-	8.0	-	-	10	-	11		
		-	8.0	-	-	10	-	11		
I <sub>NN</sub>	Average V <sub>NN</sub> supply current	-	13	-	-	14	-	16	mA	All output switches are turning ON and OFF at 50kHz with no load
		-	8.0	-	-	10	-	11		
		-	8.0	-	-	10	-	11		
I <sub>DD</sub>	V <sub>DD</sub> supply current	-	0.1	-	-	0.1	-	0.1	mA	V <sub>DD</sub> = 5.0V@ 50kHz CW
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current	-	10	-	-	10	-	10	μA	All logic inputs are static
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---

\* See Test Circuits on page 5

**AC Electrical Characteristics** (Over recommended operating conditions unless otherwise specified)

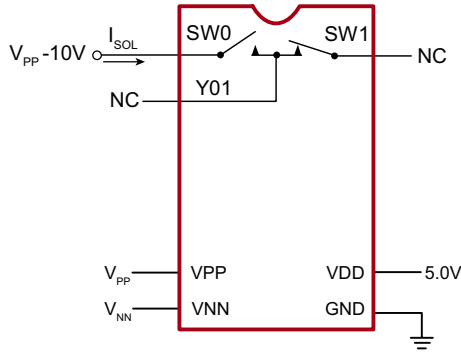
Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t <sub>ON</sub>	Turn ON time	-	30	-	15	30	-	30	μs	V <sub>SIG</sub> = V <sub>PP</sub> -10V, V <sub>PP</sub> = +100V, R <sub>LOAD</sub> = 10kΩ, V <sub>NN</sub> = -100V
t <sub>OFF</sub>	Turn OFF time	-	30	-	15	30	-	30		
dv/dt	Maximum V <sub>SIG</sub> slew rate	-	20	-	-	20	-	20	V/ns	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	20	-	-	20	-	20		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	20	-	-	20	-	20		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V
K <sub>O</sub>	OFF isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ//15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load
K <sub>CR</sub>	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I <sub>ID</sub>	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
C <sub>SG(OFF)</sub>	OFF capacitance A or B to GND	-	14	-	9.0	14	-	14	pF	V <sub>SIG</sub> = 0V, f = 1.0MHz
C <sub>SG(ON)</sub>	ON capacitance A or B to GND	-	33	-	23	33	-	33	pF	V <sub>SIG</sub> = 0V, f = 1.0MHz One SW on, one SW off
	Capacitance Y to GND	-	33	-	23	33	-	33		
+V <sub>SPK</sub>	Output voltage spike SW	-	250	-	-	250	-	250	mV	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
+V <sub>SPK</sub>		-	250	-	-	250	-	250		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
+V <sub>SPK</sub>		-	250	-	-	250	-	250		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
+V <sub>SPK</sub>	Output voltage spike Y	-	250	-	-	250	-	250	mV	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
+V <sub>SPK</sub>		-	250	-	-	250	-	250		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
+V <sub>SPK</sub>		-	250	-	-	250	-	250		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V, R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	250	-	-	250	-	250		
QC	Charge injection	-	-	-	1020	-	-	-	pC	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	-	-	700	-	-	-		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	-	-	370	-	-	-		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V

\* See Test Circuits on page 5

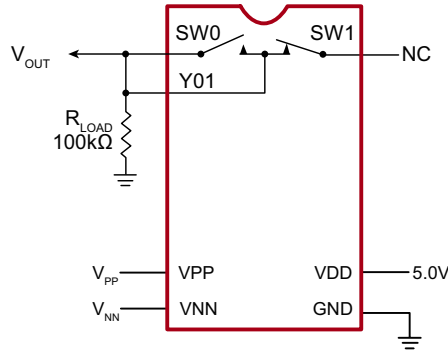
**Truth Table**

A/B	Switch Status
H	SW0, 2, 4...30 ON, SW1, 3, 5...31 OFF
L	SW0, 2, 4...30 OFF, SW1, 3, 5...31 ON

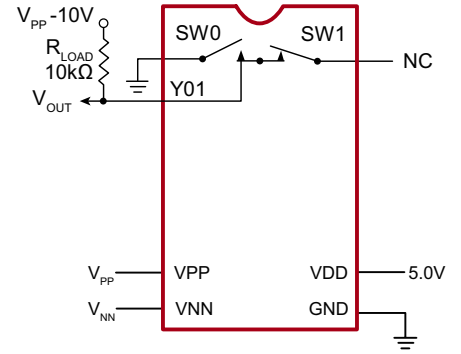
Test Circuits



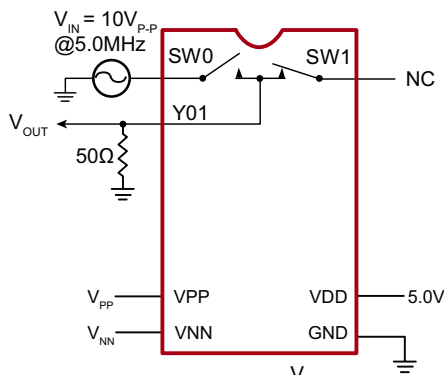
Switch OFF Leakage



DC Offset ON/OFF

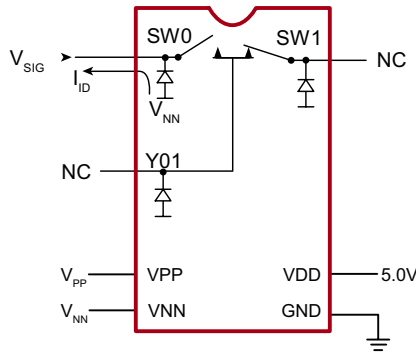


T<sub>ON</sub>/T<sub>OFF</sub> Test Circuit

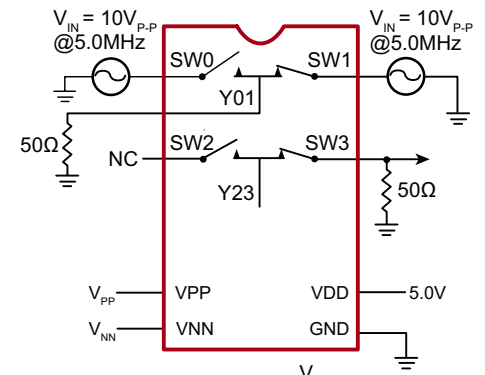


$$K_o = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

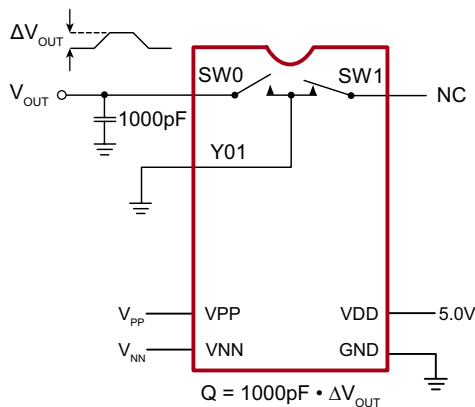


Isolation Diode Current



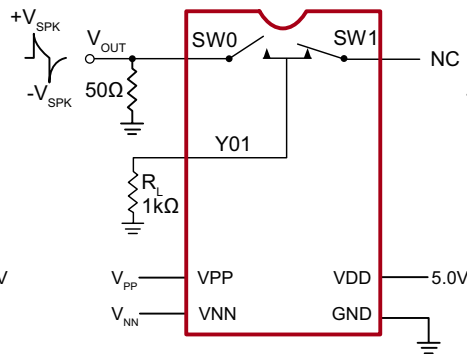
$$K_{CR} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$

Crosstalk

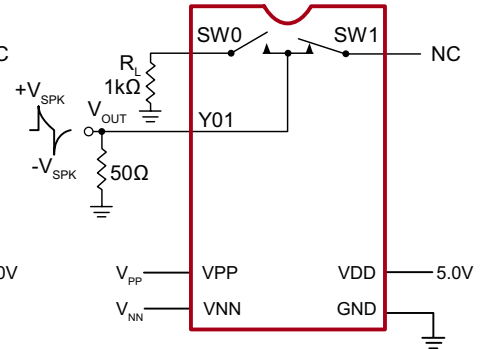


$$Q = 1000\text{pF} \cdot \Delta V_{OUT}$$

Charge Injection



Output Voltage Spike SW



Output Voltage Spike Y

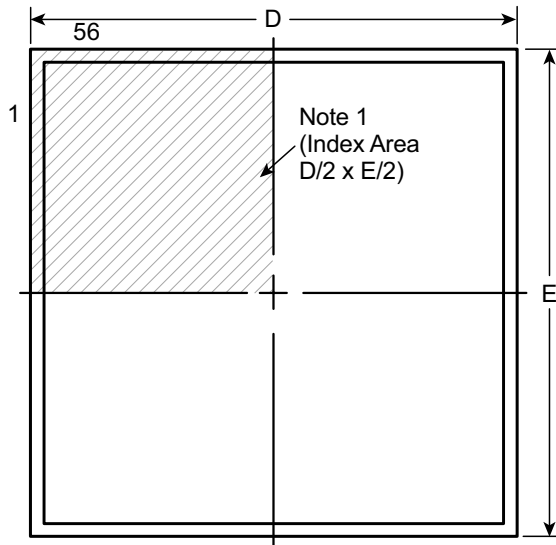
## Pin Function

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Y2829	15	SW3	29	Y1213	43	SW19
2	SW29	16	SW4	30	SW13	44	SW20
3	SW30	17	Y45	31	VNN	45	Y2021
4	Y3031	18	SW5	32	SW14	46	SW21
5	SW31	19	SW6	33	Y1415	47	SW22
6	NC	20	Y67	34	SW15	48	Y2223
7	VDD	21	SW7	35	VPP	49	SW23
8	A/B	22	SW8	36	VPP	50	SW24
9	GND	23	Y89	37	SW16	51	Y2425
10	SW0	24	SW9	38	Y1617	52	SW25
11	Y01	25	SW10	39	SW17	53	SW26
12	SW1	26	Y1011	40	VNN	54	Y2627
13	SW2	27	SW11	41	SW18	55	SW27
14	Y23	28	SW12	42	Y1819	56	SW28

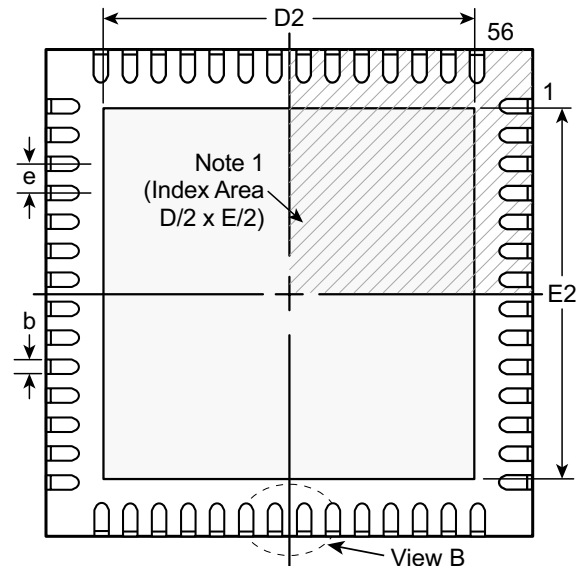
VSUB (Thermal Pad)	The central thermal pad on the bottom of package must be connected to VNN externally
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# 56-Lead QFN Package Outline (K6)

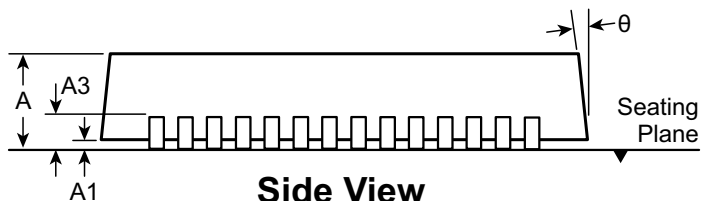
8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



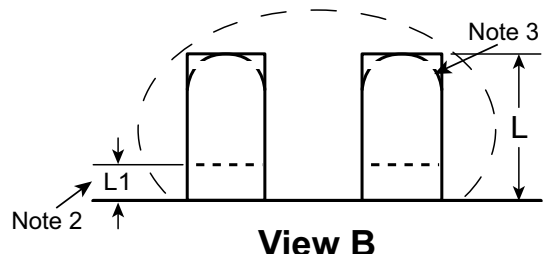
**Top View**



**Bottom View**



**Side View**



**View B**

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-56QFNK68X8P050, Version A031010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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