14W Off-line LED Driver, 120VAC, PFC, 14V, 1.0A Load

Specifications

Parameter	Value
AC line voltage	100 - 135VAC
LED (string) voltage	0 - 14V
LED current	1.0A
Switching frequency	70 - 120kHz
Efficiency	74% (@ 14V)
Open circuit protection	Yes (output voltage 33V)
Short circuit protection	Yes (output current 1.0A)
AC line undervoltage	LED and AC line current fall off gradually below 100 VAC
Light dimmer compatible	No
THD	~16% (LED voltage 14V)
Power factor	>95% (LED voltage 14V)

General Description

This Design Note describes the results of a 14W LED Driver Design. The design specifically forgoes the use of electrolytic capacitors, which form a point of weakness in high reliability and high ambient temperature applications.

The design drives one or more high brightness LEDs, in parallel or series combinations, at a current of 1.0A and up to a voltage of 14V. This same design can be operated at lower voltage/power levels as well, with slight loss of efficiency and THD.

The results, in particular the waveforms, documented in this note apply more broadly, i.e. at other output currents and voltage levels when appropriate adjustments are made to the size and value of certain components.

Efficiency can be increased by using components having less ohmic resistance, particularly L1 and M1, and by lowering the switching frequency.

The input line current features low harmonic distortion, satisfying the requirements of EN 61000-3-2 Class C (Lighting Equipment). Open circuit and in short circuit at the output can be sustained indefinitely. The AC line current is limited to an input voltage range from zero to 135VAC. Both the output current and line current drop gradually as AC line voltage falls below 100VAC.

Please refer to application note AN-H52 for a detailed description of and design guidance for the HV9931LED driver control IC.

Miscellaneous Notes

EMI, Common Mode Filtering:

The magnitude and frequency dependency of the common mode current on the line input depends heavily on physical layout and location of the LED driver circuit and the attached load. As such, the design may or may not require the addition of a common mode choke ahead of the bridge rectifier.

Open Circuit Operation

During open circuit operation the HV9931 is made to run at minimum duty cycle through the action of CS2 and ZOV. Some energy transfer, as small as it may be, still occurs, which causes the voltage on C1, and thereby the peak drain voltage on M1, to rise to a higher level. Circuit losses keep this raise in check. From experimental data: peak V_{C1} rises by about 35V from 120 to 155V, and maximum V_{DS} rises by 60V from 270 to 330V. If this rise is undesirable, a zener diode or a bleeder resistor can be placed across C1 to limit the voltage rise across C1 and M1, or more sophisticated circuitry can be added to further limit switching activity.

M1 Turn Off

An external pull down transistor was added to the gate drive circuit to speed up the turn off transition. Note that M1's drain current, which is more or less triangular in shape, is largest at turn off. Figures 19 and 20 illustrate the gain in turnoff speed that can be attained by this simple addition.

Measurements showed an increase in efficiency by 0.5% from 73.2 to 73.7%, corresponding to a reduction in switching loss of 100mW. The small gain in efficiency may not warrant the addition of the pull down transistor, but may nevertheless be interesting when power levels are higher or a larger MOSFET having more gate and reverse transfer capacitance is in use.

V_{DD} at Zero Crossing

V_{DD} may drop out at the AC line zero crossings, and cause a short lived drop in LED current if the capacitor at the VDD pin is made small. If this effect is undesirable, then the C_{DD} should be chosen sufficiently large. Figures 5 and 6 demonstrate this effect.

CS1 Programming

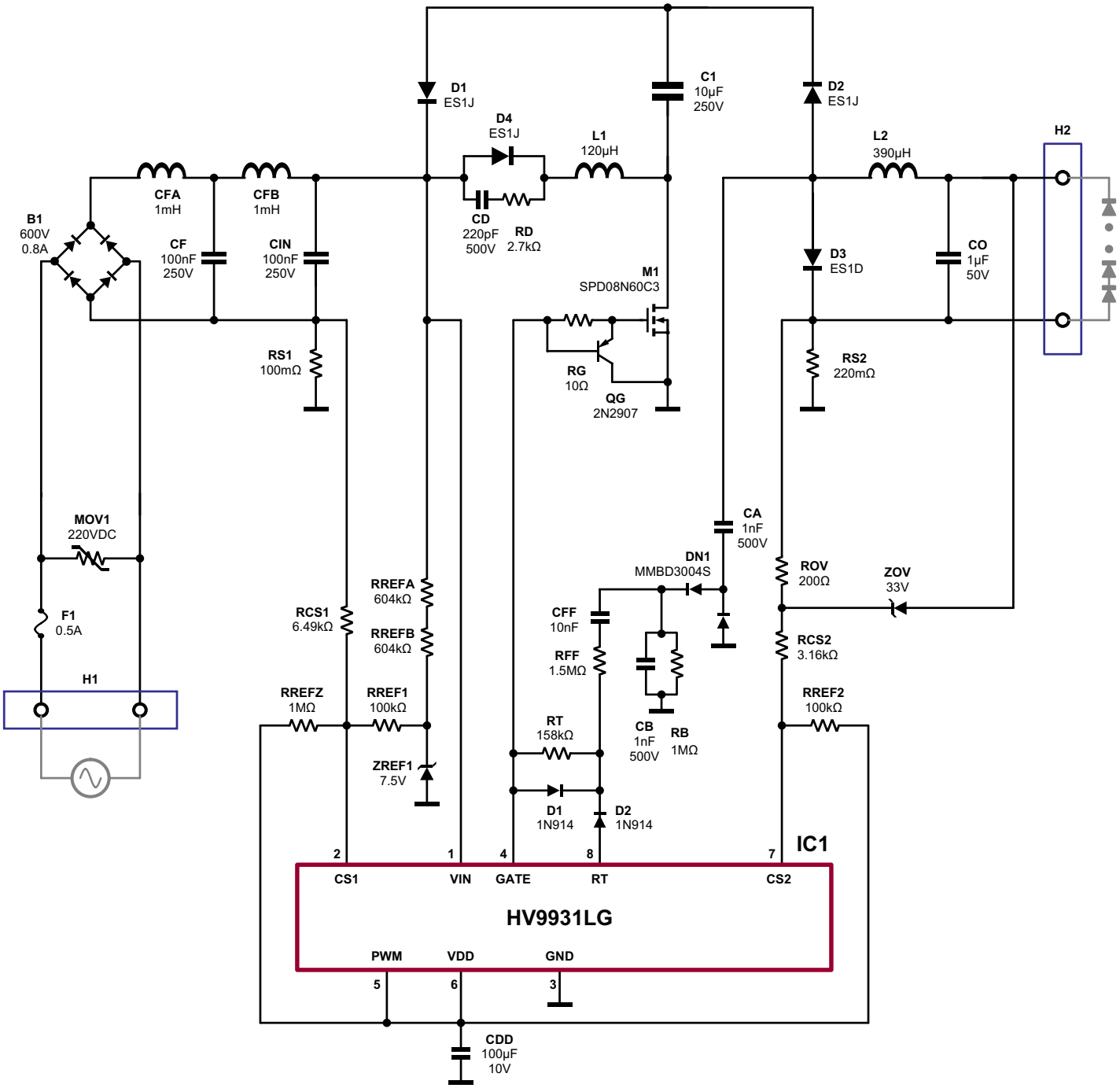
Control of M1 should, under regular circumstances, be governed by the action of comparator CS2, which provides regulation of the LED current. CS1 should regulate only if limitation of input stage current is necessary, as during AC line undervoltage or during transient conditions. CS1 is to remain inactive by programming an envelope for the input stage current with an adequate margin, such that CS1 does not interfere with the regulation of the output current under normal circumstances. A simple DC threshold of adequate value will suffice.

This design employs a somewhat more sophisticated envelope for the purpose of limiting the AC line current when undervoltage occurs. The threshold is a scaled version of the input voltage, thus reducing input current as input voltage reduces. By proper choice of values, CS1 will thus become active for input voltages lower than 100VAC, and take over regulation by limiting input stage current to an approximate sinusoidal waveform. For line voltages larger than 100V, this scaled threshold will become unnecessarily accommodative, and zener diode Z_{REF1} will limit its rise.

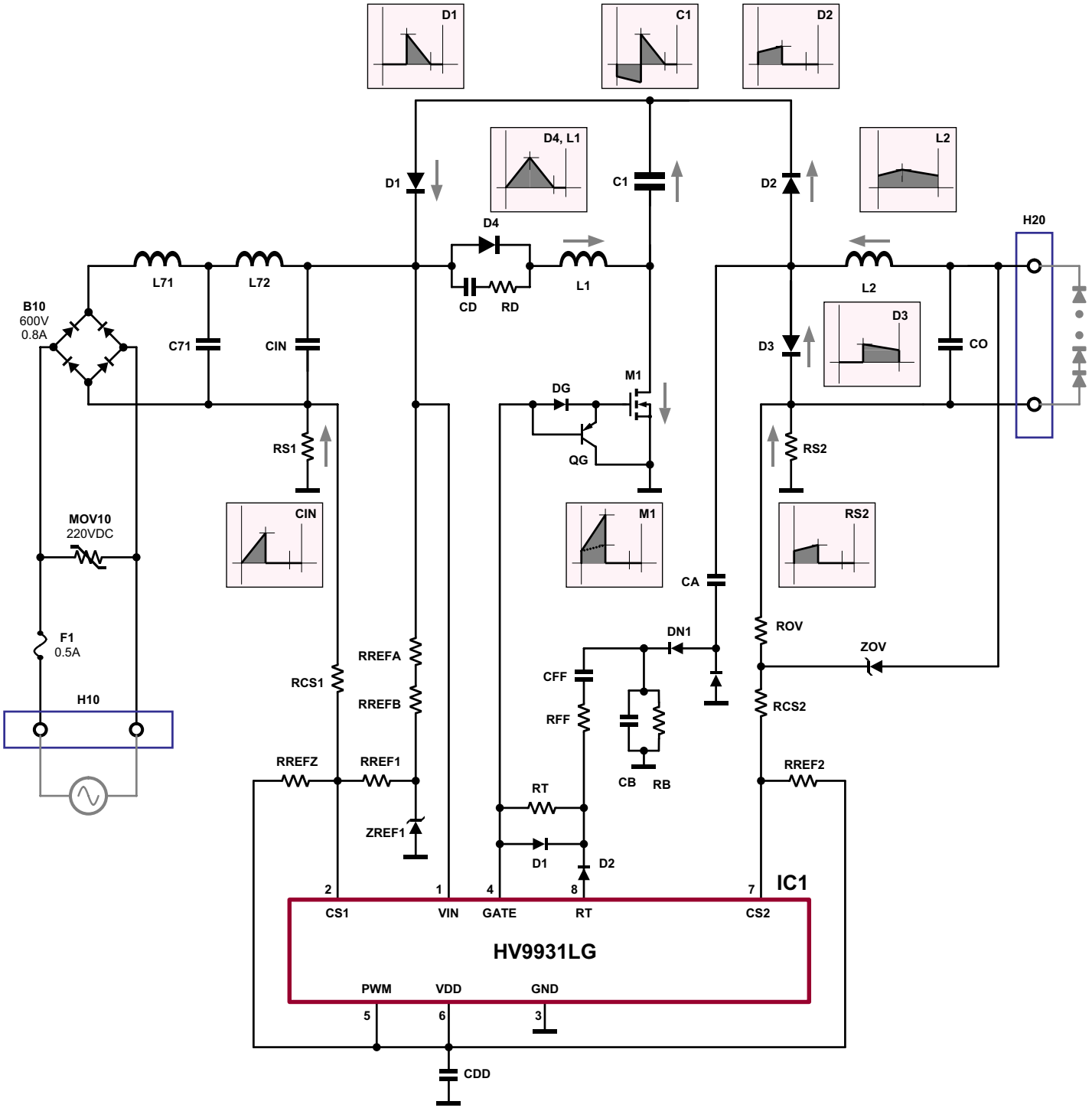
Diodes D1 and D2

D1 and D2 are part of the RT oscillator circuit which determines the switching frequency, or more precisely, the off-time (T_{OFF}) of the switching period. The off time is determined by the oscillator discharge current which should appear when M1 is turned off, i.e. when the GATE pin is low. The main contribution to the discharge current is due to current in RT when the voltage at the GATE pin is low. Current originating at the RFF resistor is meant to modulate this discharge current in order to affect an increase or decrease of T_{OFF}. Note that RFF is driven by the ripple voltage across C1. As such, RFF carries an alternating current, which is present regardless of the timing needs of the RT pin. D1 and D2 resolve two issues depending on the polarity of the RFF current. When RFF sources current, it will overdrive the pin when GATE is high, which is undesirable. Diode D2 blocks this current, and the current will follow an the path through RT and the GATE pin. When RFF sinks current, diode D1 sources this current during the time that the RT discharge current should be zero (GATE pin high).

Schematic 1


D1
ES1J
D4
ES1J
L1
120µH
C1
10µF
250V
D2
ES1J
L2
390µH
H2
CFA
1mH
CFB
1mH
B1
600V
0.8A
CF
100nF
250V
CIN
100nF
250V
CD
220pF
500V
RD
2.7kΩ
M1
SPD08N60C3
D3
ES1D
CO
1µF
50V
RS1
100mΩ
RG
10Ω
QG
2N2907
RS2
220mΩ
MOV1
220VDC
CA
1nF
500V
DN1
MMBD3004S
ROV
200Ω
ZOV
33V
F1
0.5A
RREFA
604kΩ
RCS1
6.49kΩ
RREFB
604kΩ
CFF
10nF
RFF
1.5MΩ
RCS2
3.16kΩ
H1
RREFZ
1MΩ
RREF1
100kΩ
CB
1nF
500V
RB
1MΩ
RREF2
100kΩ
RT
158kΩ
ZREF1
7.5V
D1
1N914
D2
1N914
IC1
2
1
4
8
7
CS1
VIN
GATE
RT
CS2
HV9931LG
PWM
VDD
GND
5
6
3
CDD
100µF
10V

Schematic 2


D1
C1
D2
D4, L1
L2
H20
D4
L71
L72
L1
L2
B10
600V
0.8A
CD
RD
D3
C71
CIN
CO
M1
DG
QG
RS1
RS2
MOV10
220VDC
CA
F1
0.5A
DN1
ROV
ZOV
RREFA
RCS1
CFF
RFF
RREFB
CB
RB
RCS2
RREFZ
RREF1
RREF2
RT
ZREF1
D1
D2
IC1
2
1
4
8
7
CS1
VIN
GATE
RT
CS2
HV9931LG
PWM
VDD
GND
5
6
3
CDD

Schematic 3

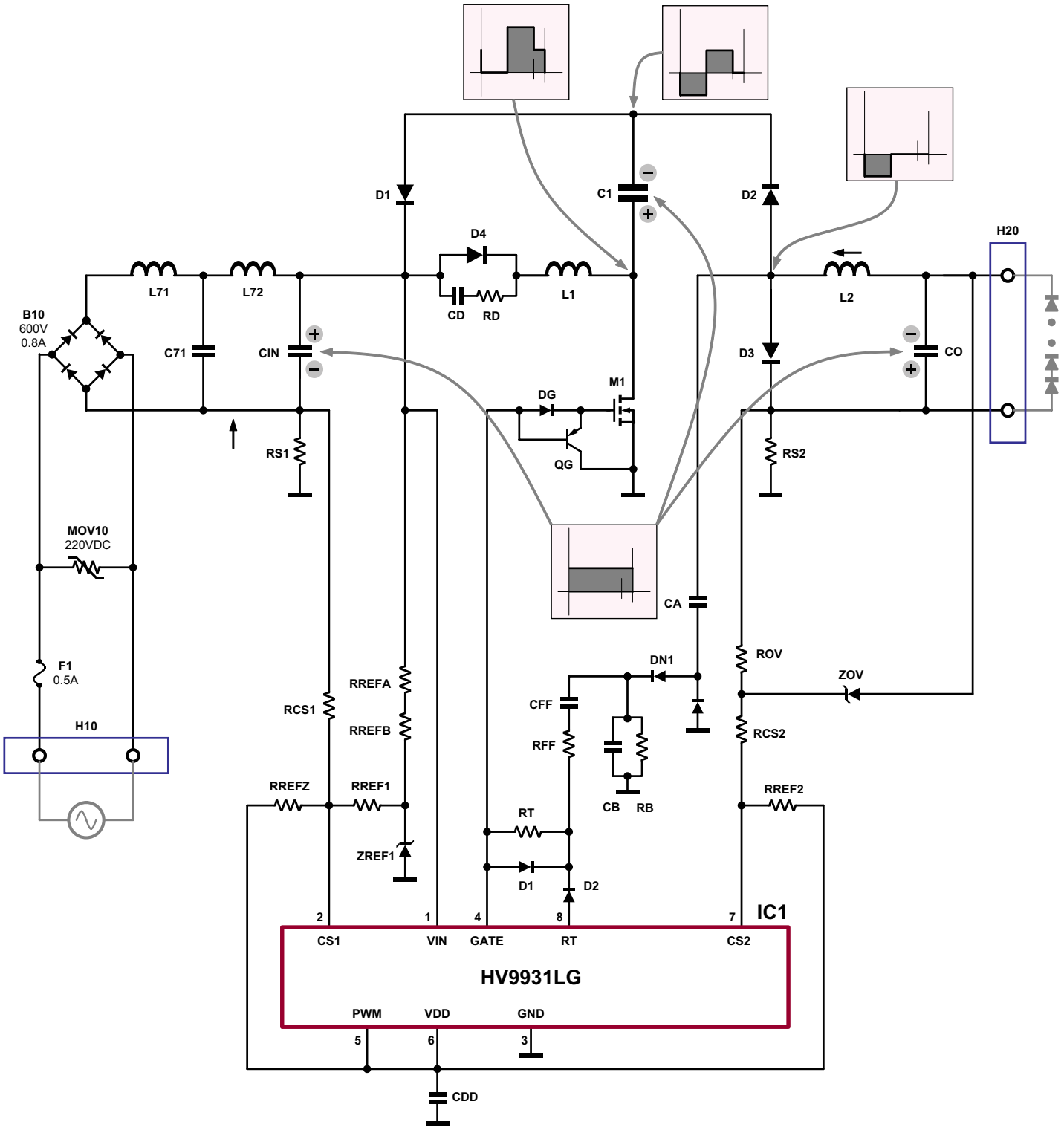
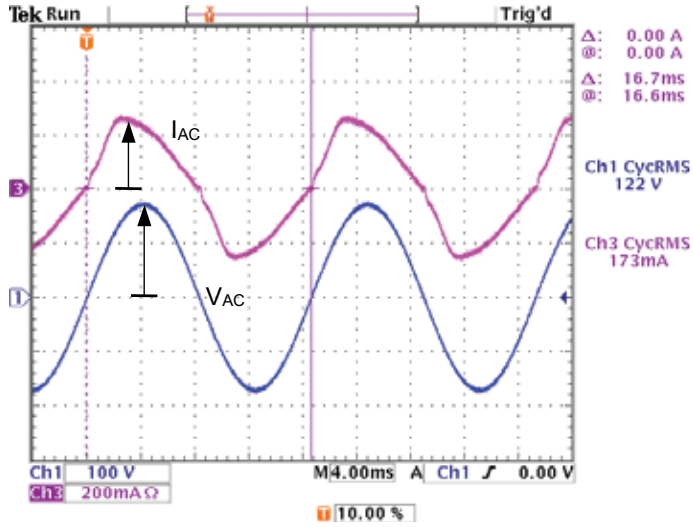
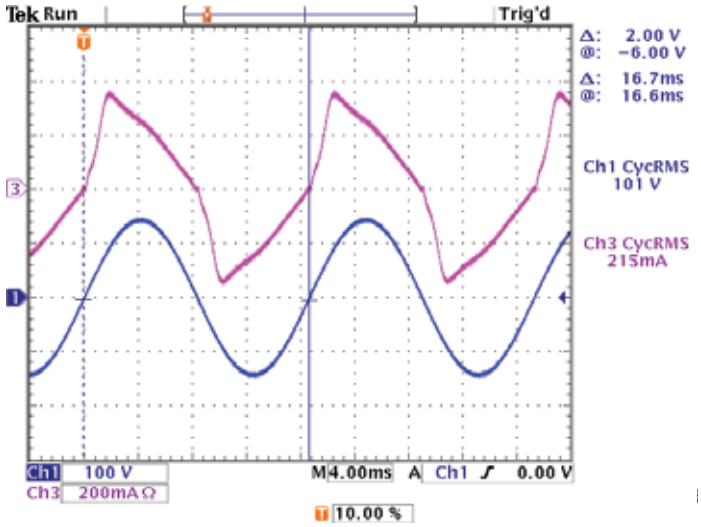

D1
C1
D2
D4
H20
L71
L72
CD
RD
L1
L2
B10
600V
0.8A
C71
CIN
D3
CO
DG
M1
QG
RS1
RS2
MOV10
220VDC
CA
F1
0.5A
H10
DN1
ROV
ZOV
RCS1
RREFA
RREFB
CFF
RFF
RCS2
CB
RB
RREFZ
RREF1
RREF2
RT
ZREF1
D1
D2
IC1
2
1
4
8
7
CS1
VIN
GATE
RT
CS2
HV9931LG
PWM
VDD
GND
5
6
3
CDD

Fig 1. (V_{AC}, I_{AC}), Nominal (120V)



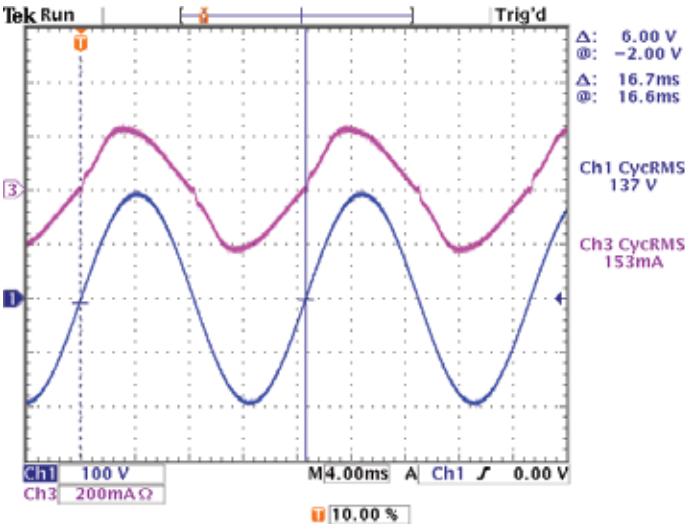
THD: 15.3%

Fig 2. (V_{AC}, I_{AC}), Low Line (100V)



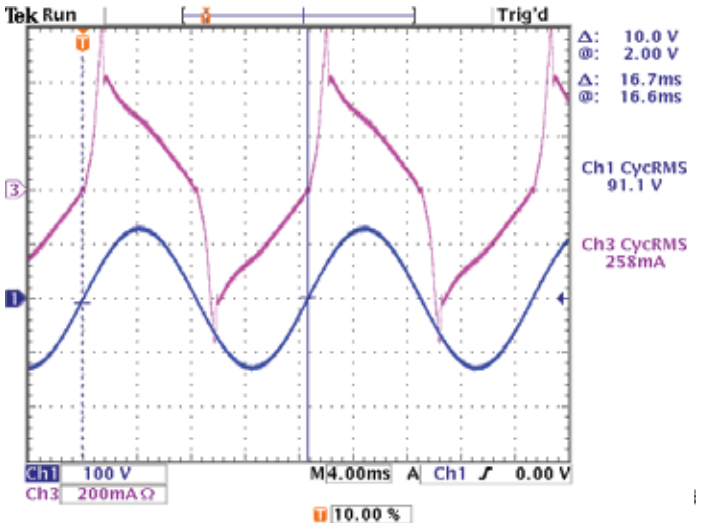
THD: 22.5%

Fig 3. (V_{AC}, I_{AC}), High Line (135V)



THD: 9.2%

Fig 4. (V_{AC}, I_{AC}, Undervoltage (90V)



THD: 35.6%

Fig 5. (V_{DD}, I_{LED}) with Large C_{DD} (100µF)

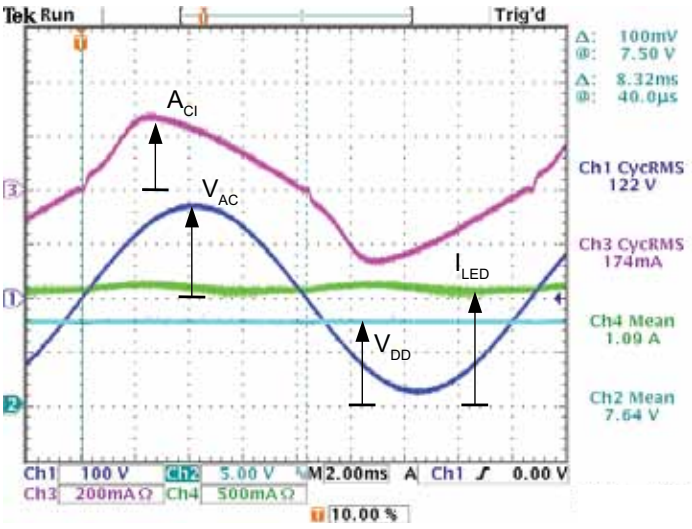
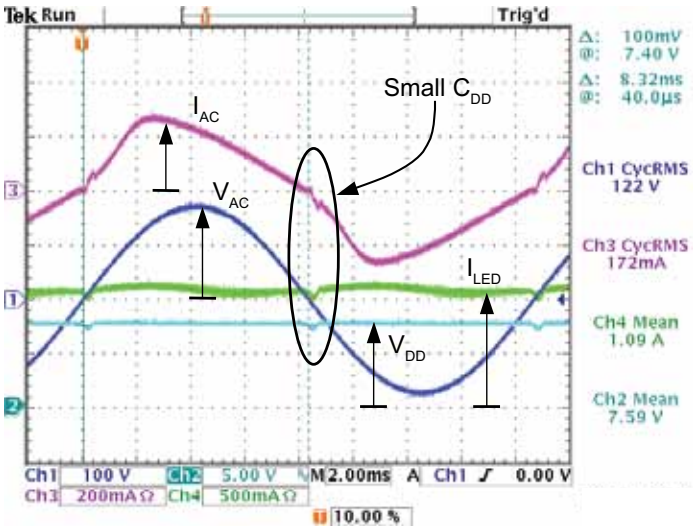
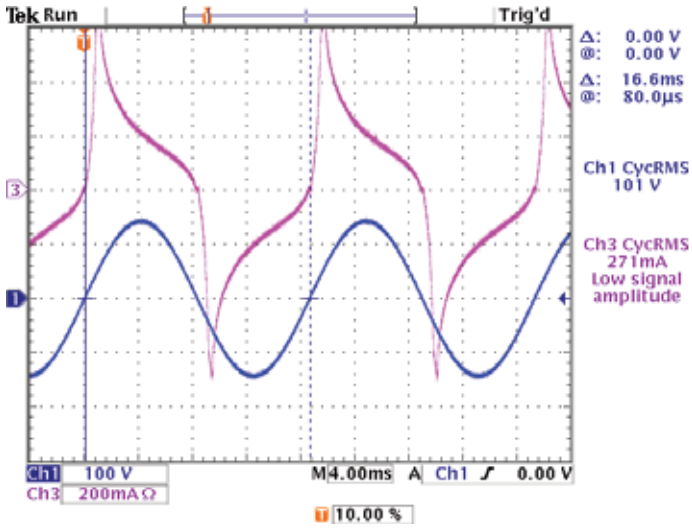


Fig 6. (V_{DD}, I_{LED}) with Small C_{DD} (1µF)



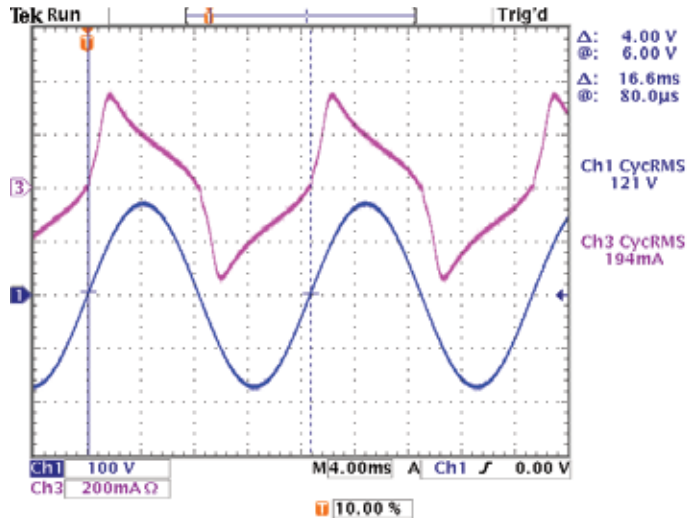
Much smaller C_{DD} is feasible, if slight loss of regulation at the zero crossings is acceptable.

Fig 7. (V_{AC}, I_{AC}), R_{FF} Removed, Low Line



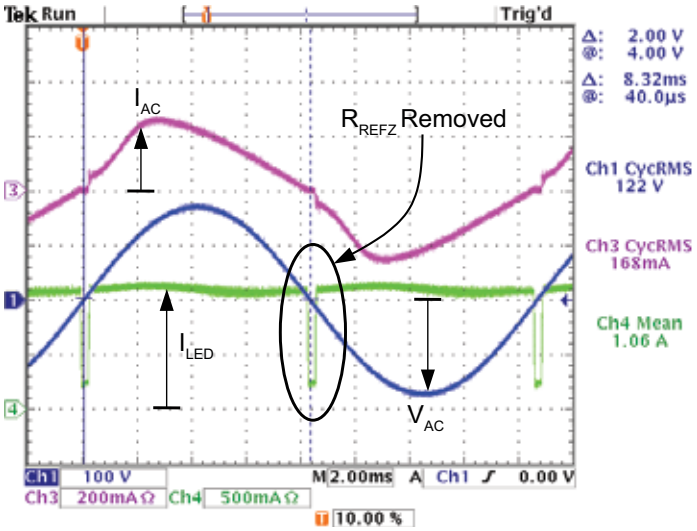
THD: Increases to 54.1% (from 22.5%)

Fig 8. (V_{AC}, I_{AC}), R_{FF} Removed, Nominal



THD: Increases to 31.5% (from 15.3%)

Fig 9. (I_{LED}, I_{AC}, V_{AC}) when R_{REFZ} Removed



R_{REF3} is needed to prevent loss of I_{LED} regulation at the zero crossings, where CS1 not receive adequate bias from V_{IN}.

Fig 10. (V_{IN}, V_{C1}, I_{L1}) Detail, (2ms/div)

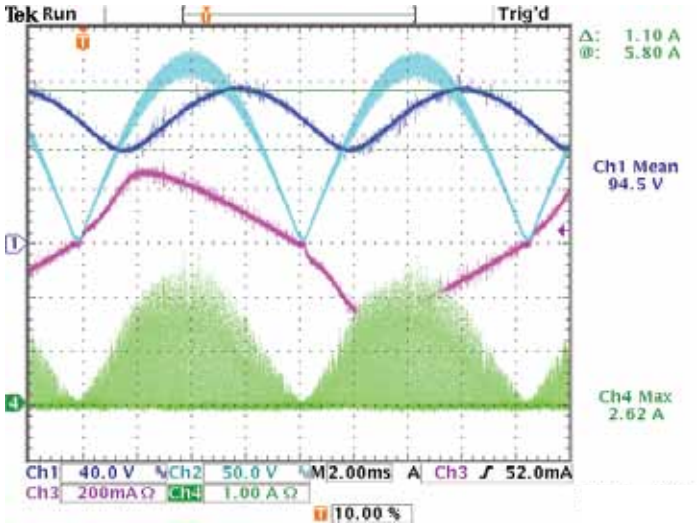


Fig 11. (V_{IN}, V_{C1}, I_{L1}) Detail, (1ms/div)

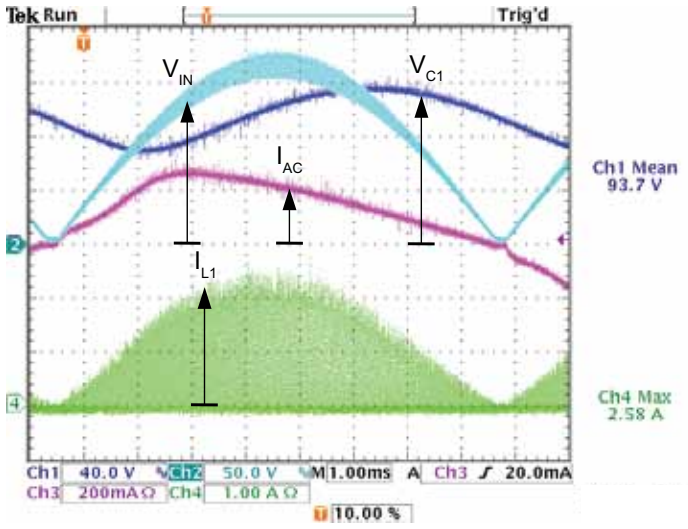


Fig 12. (V_{IN}, I_{AC}, I_{L1}) Detail, (100µs/div)

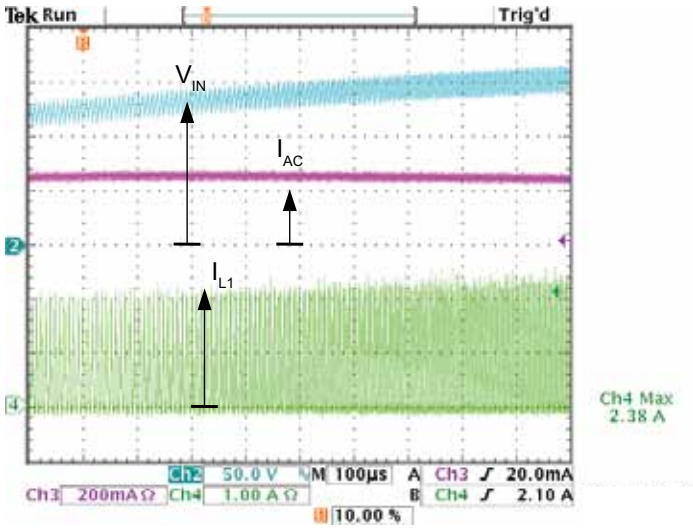


Fig 13. (V_{IN}, I_{AC}, I_{L1}) Detail, (10µs/div)

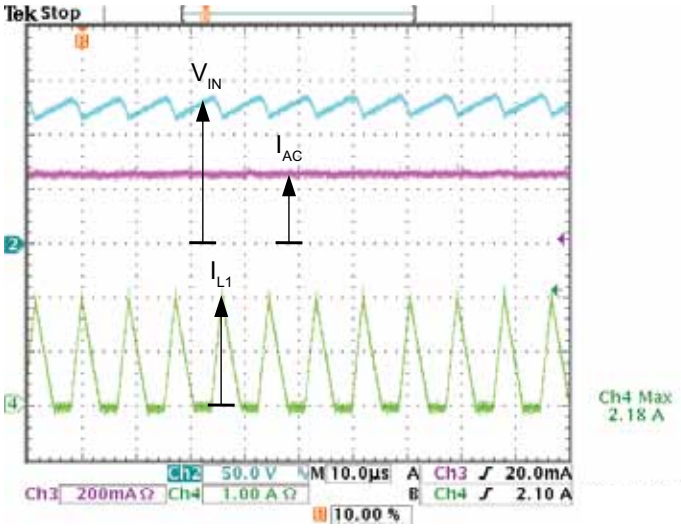


Fig 14. (V_{IN}, I_{AC}, I_{L1}) Detail, Time Base (2µs/div)

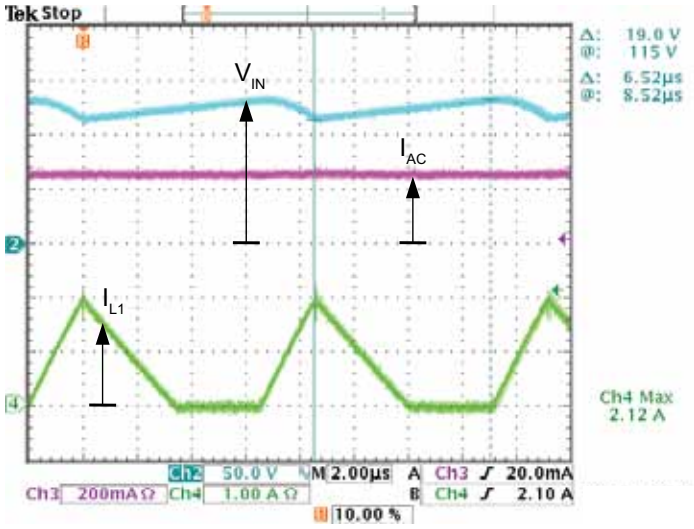


Fig 15. M1 Drain Voltage, (2µs/div)

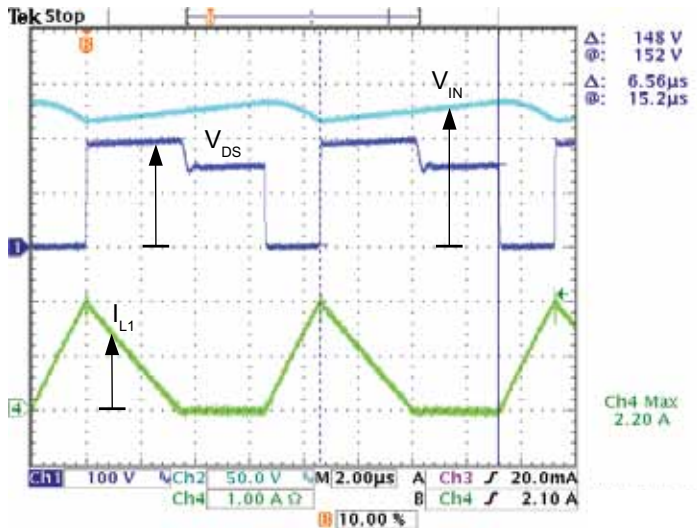


Fig 16. M1 Drain Voltage, (20µs/div)

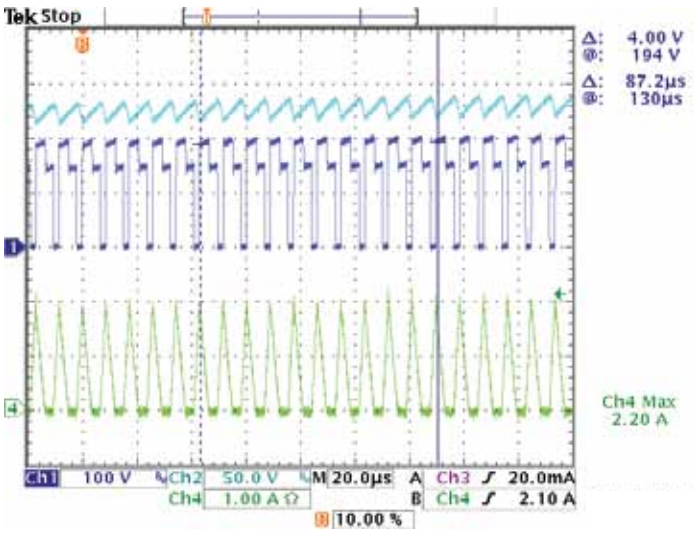


Fig 17. M1 Drain Voltage, (2ms/div)

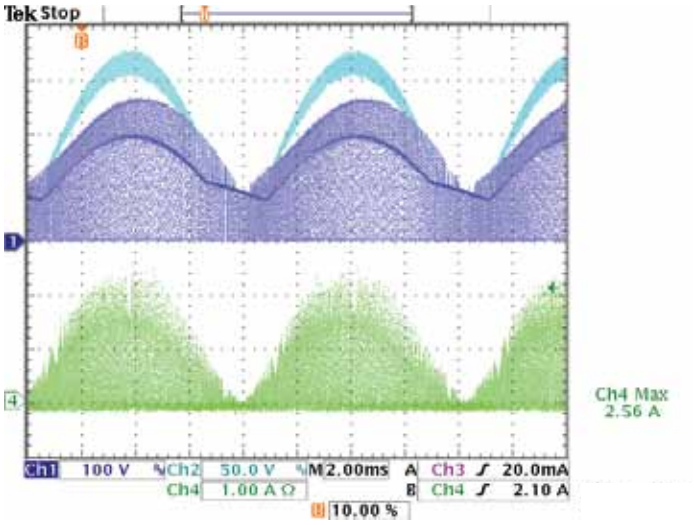
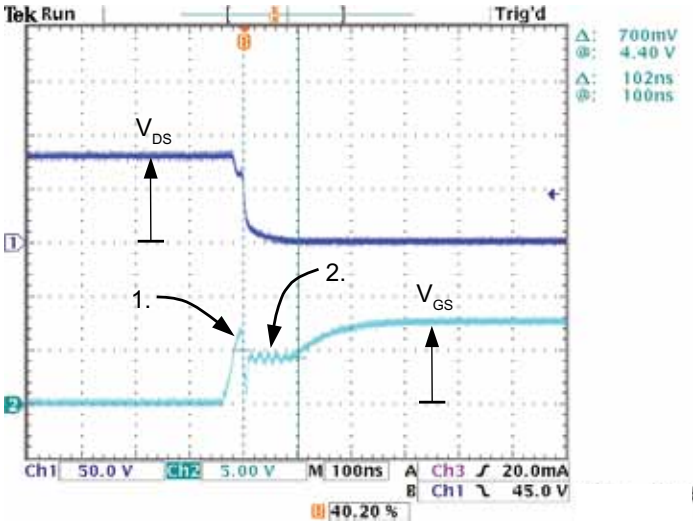
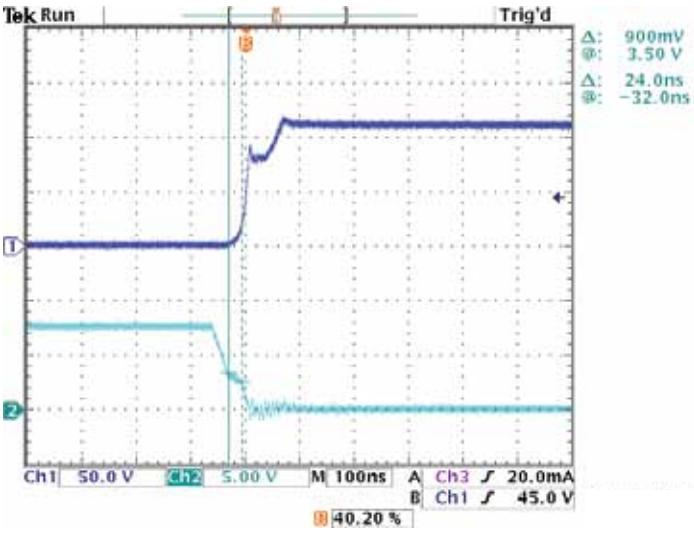


Fig 18. M1 Turn on



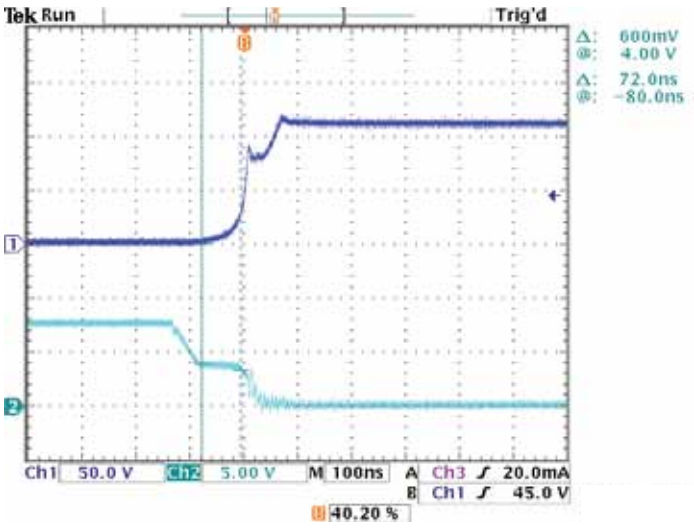
1. V_{GS} *rises steadily; Diode D3 recovers.*
2. V_{GS} *plateaus; Miller effect due to falling* V_{DS}.

Fig 19. M1 Turn Off



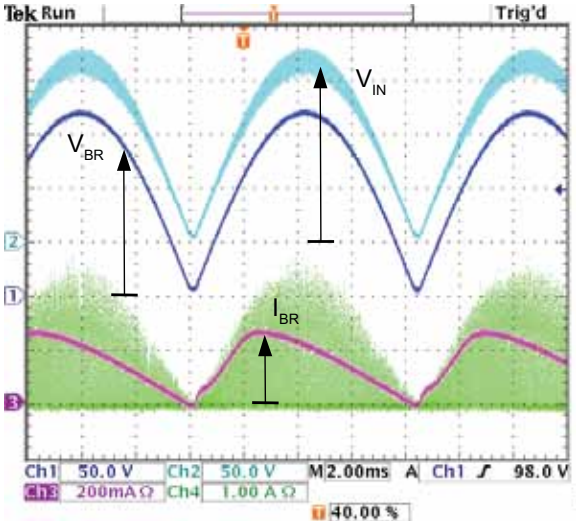
V_{GS} plateau about 25ns.
Gate turn-off assisted by external PNP pull down transistor

Fig 20. M1 Turn Off, Q1 Removed



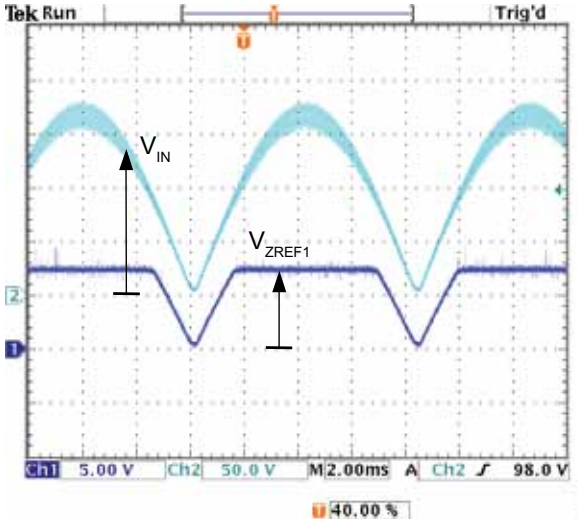
Slower turn-off. V_{GS} plateau about 70ns.
Pull down transistor Q1 removed, and ZeroΩ RG.

Fig 21. Input Filter Detail, (V_{IN}, V_{BR}, I_{BR})



No ripple visible on V_{BR}: Filter rejects voltage ripple of V_{IN}.
No Ripple visible on I_{BR}: Filter rejects current ripple of I_{L1}.

Fig 22. CS1 Programming Detail, V_{ZREF1}



Limit defined in part by DC level, in part by V_{IN}.
Limit never exceeds DC level,

Fig 23. Line Regulation

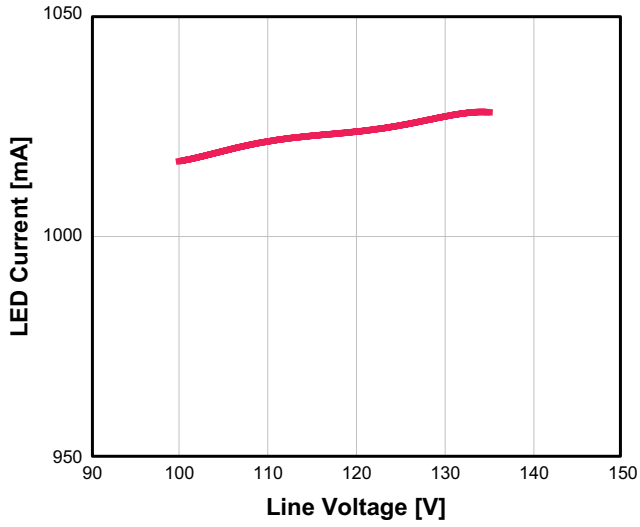


Fig 24. Efficiency vs Line Voltage

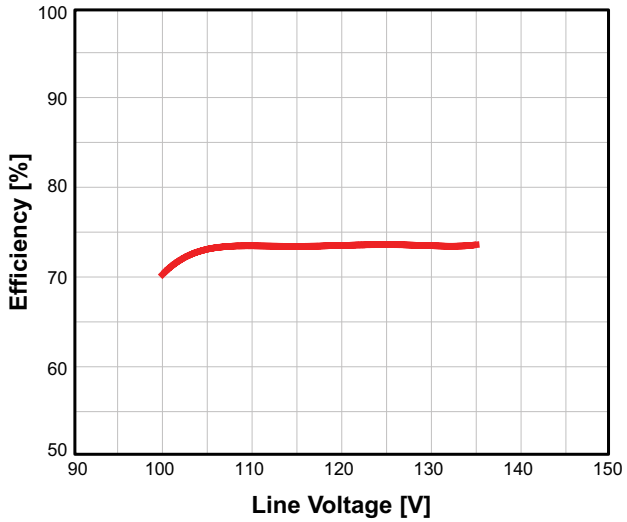


Fig 25. THD vs Line Voltage

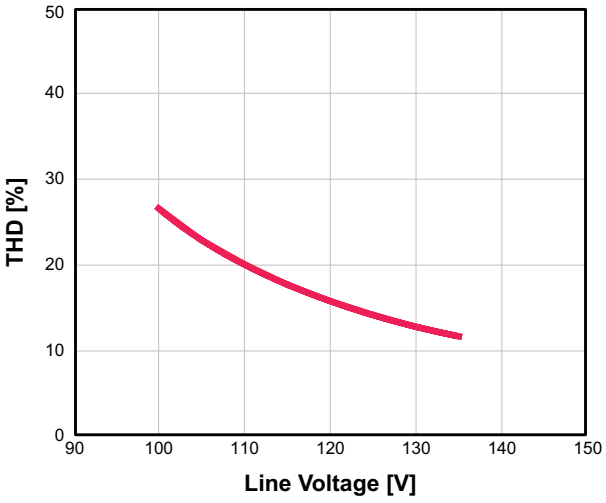


Fig 26. Power Factor vs Line Voltage

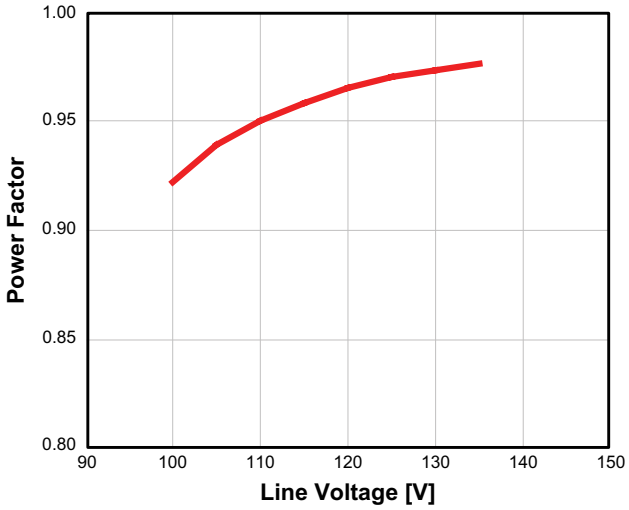


Fig 27. Load Regulation

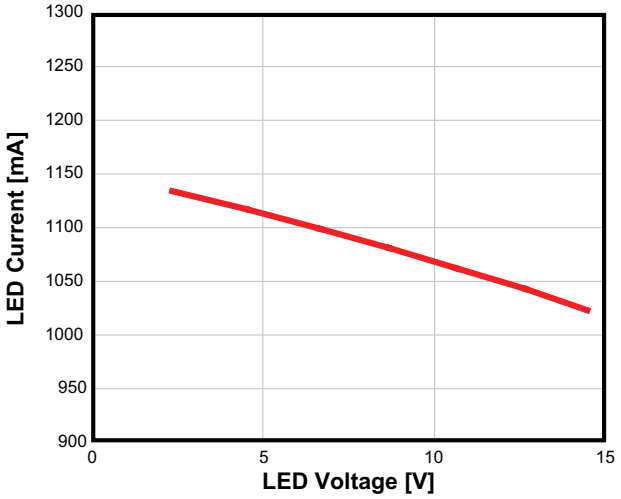


Fig 28. Efficiency vs Load Voltage

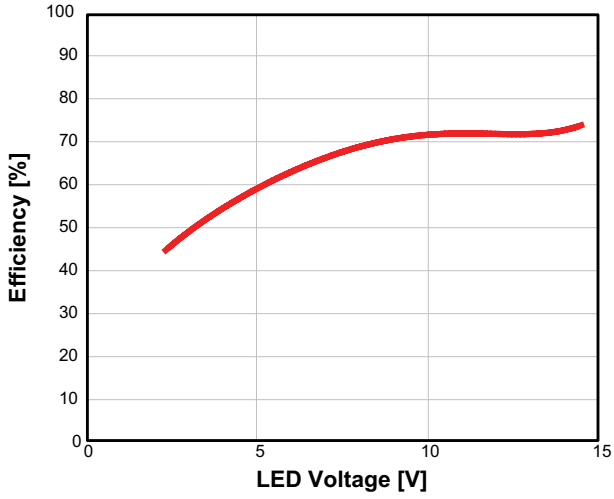


Fig 29. THD vs Load Voltage

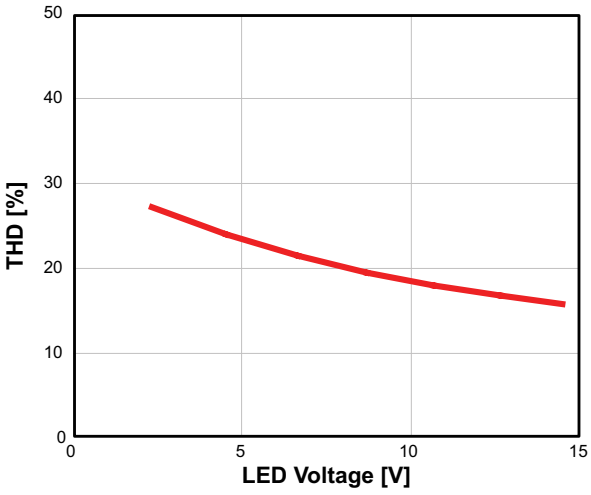
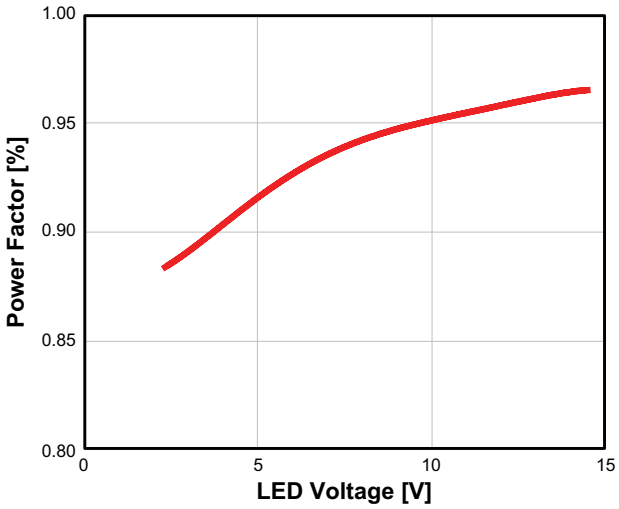


Fig 30. Power Factor vs Load Voltage



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