Charting a HV9931 Driver Design

This application note allows you to generate or check a HV9931 based driver design by using a set of graphs and scaling rules. The graphs describe a base design for a range of possible output voltages. Simple scaling rules allow you to adapt the graphical data to the output current and switching frequency of your target design. The driver design features AC input with power factor correction, satisfying IEC harmonic limits for lighting equipment (EN61000-3-2 Class C).

Please refer to application note AN-H52 for detailed information on HV9931 based LED Driver design. The data presented here is a graphical representation of the information given in AN-H52.

Graphs are attached for the following three common design cases:

1. 120VAC input (85V…135V)
2. 240VAC input (200V…265V)
3. Universal input (85V…265V)

The graphs represent design data, such as component values, stress ratings, duty cycle, etc for a driver design at an output voltage of your choice (up to 100V). As higher output voltage represents higher output power, choose the lowest output voltage compatible with your needs. Read the design data from the curves and enter the values into the associated worksheet on the next page. These values correspond to a base design with 1A of output current and an off-time of 10µs.

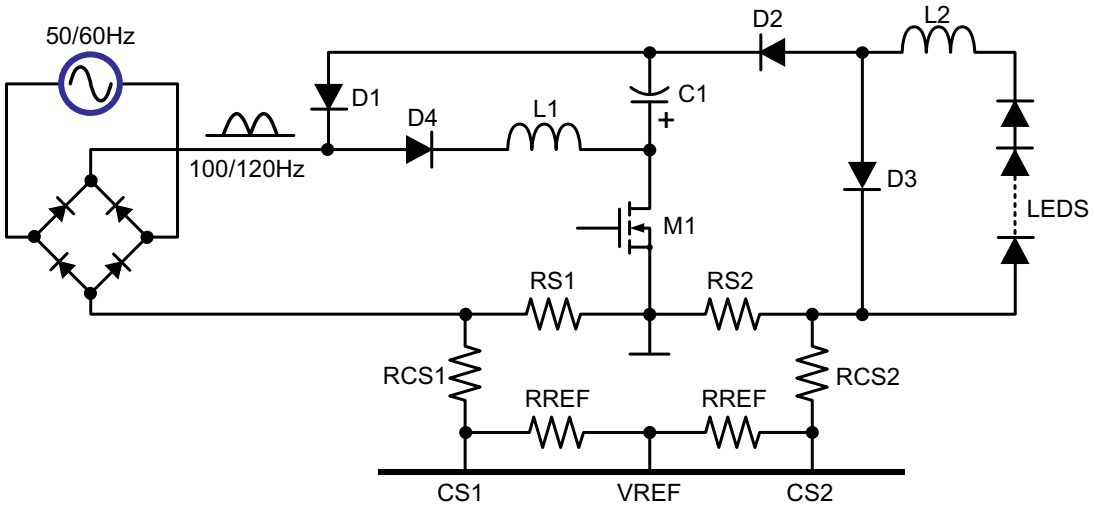
The worksheet contains a sample design for your guidance. Subsequently, scale the base design data to the desired output current and off-time of your target design. The worksheet contains the scaling instructions for all parameters; either multiply (M), divide (D) or leave the parameter unchanged (✓) using the ratio of target current and target T-off time. A sample calculation for a target of 500mA and 15µs is provided in the worksheet.

Supplementary specifications of the base design are as follows:

- Estimated Efficiency: 75%.
- Output Current Switching Ripple: 30%.
- Input Current 3rd Harmonic: 10%.
- AC Line Frequency: 50Hz (240V); 60Hz (120V); 50Hz/60Hz (Universal).
- RS1, RS2 Trip Voltage: 500mV.
- RREF: 100kΩ.

The graphs provide design information on the:

- Components: (L1, L2, C1), (M1, D1, D2, D3, D4), (RS1, RCS1, RS2, RCS2)
- Timing: Duty Cycle, Switching Frequency
- AC line: Line Current, Line Power



Hints and Comments

Input Voltage Range:

The base design will operate at voltages higher than 135V (265V) without major change. The voltage ratings of the MOSFET, the diodes and C1 should be increased accordingly.

Input Voltage Range, Lower Input Voltage:

Operation at input voltages lower than 85V (200V) is possible as well. This requires lowering of the inductance of L1 in order to avoid continuous current mode operation of the input stage, which leads to severe input current waveform distortion (see AN-H52 for general theory of operation). Do not lower the inductance of L1 unnecessarily, as the reduction in L1 will bring about a need for higher voltage and current ratings of the power stage components. AN-H52 allows you to study the impact of this change.

L1, Nominal Range:

Stay close to the calculated value when finalizing the design. The computed value is a maximum value; using a larger value results in CCM operation at low AC line voltage, thus causing the input current to become severely distorted. Using a small value for L1 causes the current and voltage stress on a number of components to increase. Keep in mind that the standard tolerance of inductors is in the 10 to 20% range, and that therefore the nominal value of the inductor should be adjusted accordingly.

Should the initial target inductance differ considerably from commercially available inductance values, then a commercially available value can nevertheless be accommodated by adjusting the switching frequency, which is accomplished by adjusting T_{OFF}. The worksheet shows in which way L1 (and couple of other parameters) can be changed by a change in T_{OFF}.

L1, Construction:

Particular attention should be paid to the design or rating of inductor L1. Inductor L1 operates in discontinuous current mode (DCM), that is, the current swings between zero and the peak value within a single switching cycle. This large current swing at high frequency (50 … 100kHz) may cause significant losses, if not addressed properly.

The current of L1 swings 100% within a single switching cycle; in contrast, the current of L2 swings about 30%. Typically, commercially available inductors are specified with DC current ratings only, and the designer is left to guess the performance under AC conditions. A good starting point for design is to assume that the AC Rating of the inductor is four times less than its DC rating.

L1 deserves particular attention because of its high current swing. When designing inductors, the related magnetic flux density swing can be adjusted to an acceptable level by proper choice of core geometry and winding detail.

Powdered iron cores and ferrite cores have been used with success. Low cost drum core types (surface mount or leaded type) can be used as well, and are especially convenient during the prototyping stage due to their widespread availability. The ambient magnetic field of these unshielded types may induce voltage in nearby circuits and other elements casuing shift in operating point and eddy current losses. This effect can be quite noticeable, and forces placement of such inductors well away form control circuitry, copper planes, heatsinks, capacitors, etc. The ambient field can cause excessive EMI as well, which may cause non-compliance with EMI standards.

If space is at a premium, cores with a closed magnetic core or having shielding, such as toroids or EE cores should be used, which tend to be more expensive, but cause lower losses and allow tighter packaging.

Switching Frequency, Efficiency, Size:

Switching frequency can be scaled up or down based on the typical trade-offs between cost, size and efficiency. An efficiency of 75% was assumed. Higher efficiencies are attainable by lowering switching losses and conduction losses which generally means the use of larger / more expensive components.

RS2:

Note the assumed circuit location of RS2; in older schematics RS2 is located in the path between D3 and CO and thus carries the load current at all times; in newer schematics RS2 is located in the path between D3 and circuit ground and carries current only during the on-time of the MOSFET. The new location leads to significantly less power dissipation and is therefore preferred. The graph of RS2 dissipated power reflects the new circuit location.

Line Frequency:

When the line frequency differs from 60Hz (50Hz), then the capacitance of C1 should be adjusted. C1 is inversely related to the line frequency; e.g. at a line frequency of 400Hz, C1 can be 6.7 (8) times smaller. Note that the RMS Current Rating of commercially available capacitors may not allow you to fully exploit this potential reduction.

RS1, RS2:

RS1 (or RS2) can be scaled up or down to match a commercially available value; RCS1 (or RCS2) should be scaled up or down with the same factor.

A Current Threshold voltage of 500mV provides a good starting point for the majority of applications. The threshold voltage can be increased in order to lower noise sensitivity or reduce the impact of the CS1 and CS2 offset voltage, or can be decreased in order to lower sense resistor power dissipation.

Non-Electrolytic Capacitor Designs:

This procedure documents design which does not incorporate the T-off modulation technique as described in AN-H52. T-off modulation allows further reduction of AC line current harmonics, at the expense of a few (low cost) components. An alternate use of the modulation technique is reduction of C1 capacitance, while maintaining a similar level of harmonics. Reduction of capacitance on the order of five times or more is viable. The capacitance reduction may warrant replacement of an electrolytic capacitor with a film or a ceramic capacitor.

Non-electrolytic capacitors are preferable in situations where high temperature operation or long life is desired. Note that a switch to non-electrolytic capacitors does not necessarily mean that physical size reduces as well, which is an area where electrolytic capacitors excel.

Another price to pay is that less capacitance brings about an increase in the 100/120Hz ripple on the C1 capacitor, which requires corresponding increases of the voltage rating of all surrounding components. E.g., a reduction by a factor of five results in five times more 100/120Hz ripple. Note that the calculation of L1 assumes that C1 is fairly large, corresponding to a C1 voltage that is quasi DC. This assumption may not be valid anymore, and with large enough ripple, the capacitor voltage in the ripple valley may be low enough so as to cause continuous conduction mode operation during part of the AC line cycle, which is undesirable. This can be remedied by a reduction in value of L1, which increases the margin to CCM operation for a given capacitor voltage, and at the same time raises the DC operating point for the capacitor giving additional margin.

Fig. 1 - AC Line Power (W) vs Output Voltage (V)

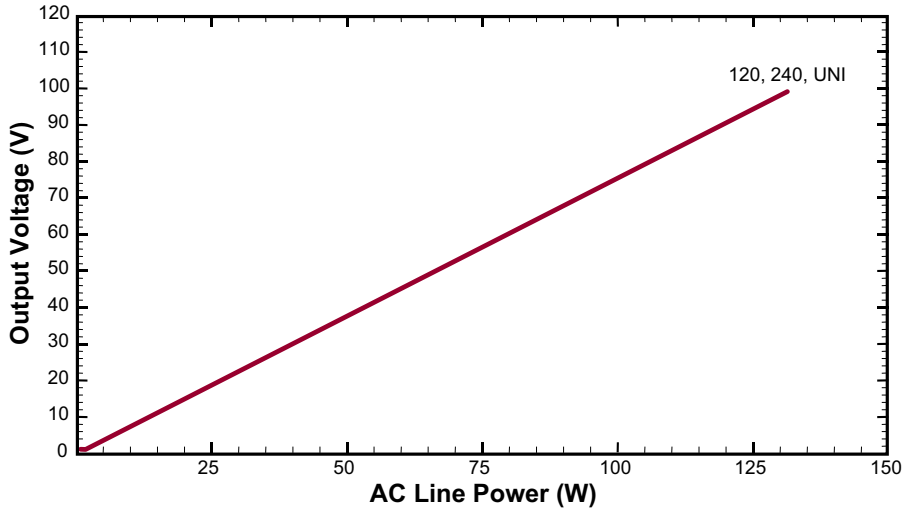


Fig. 2 - Max RMS Line Current (A) vs Output Voltage (V)

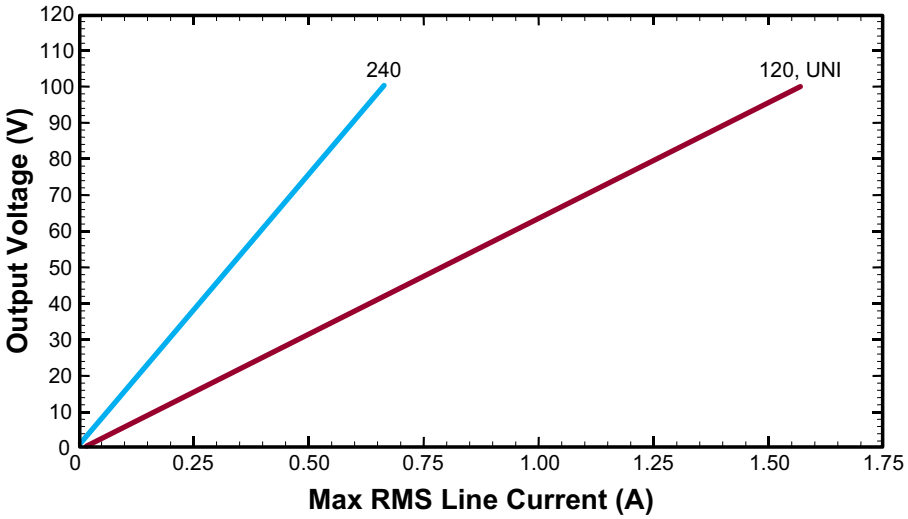


Fig. 3 - L1 Inductance (µH) vs Output Voltage (V)

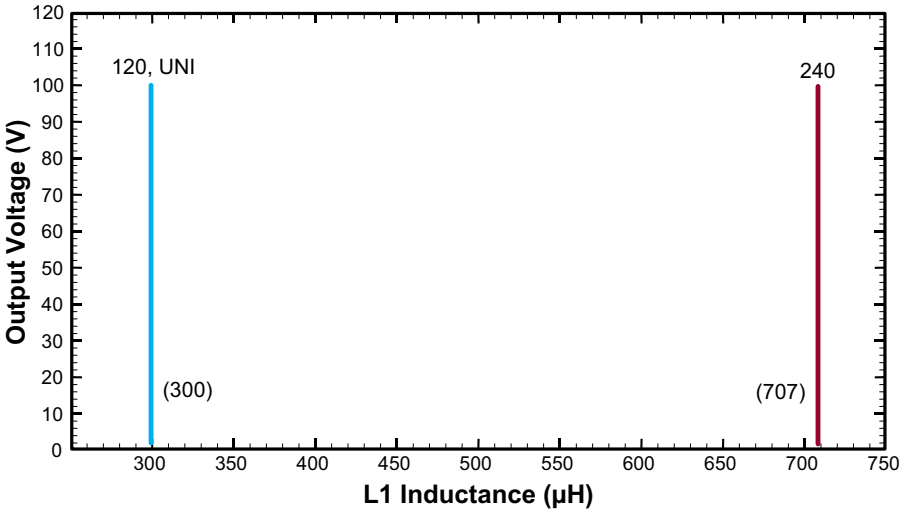


Fig. 4 - L1 Peak Current - LL (A) vs Output Voltage (V)

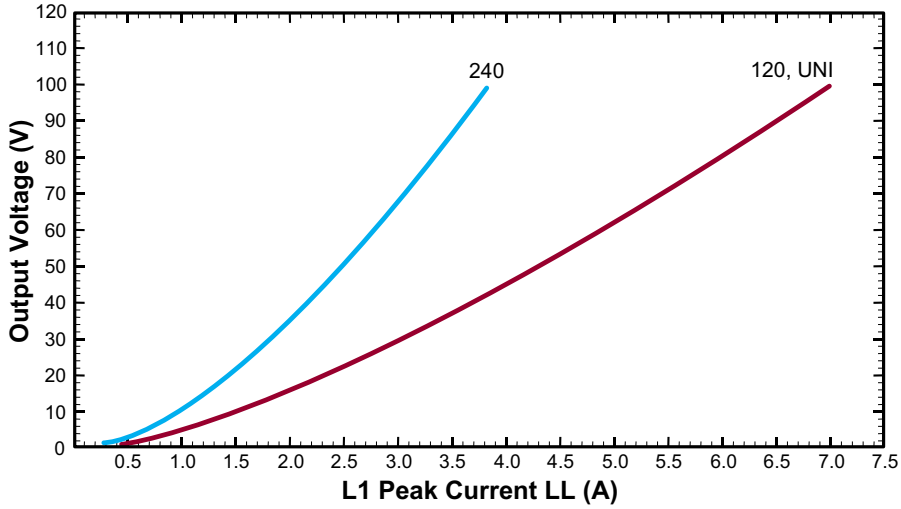


Fig. 5 - L1 RMS Current - LL (A) vs Output Voltage (V)

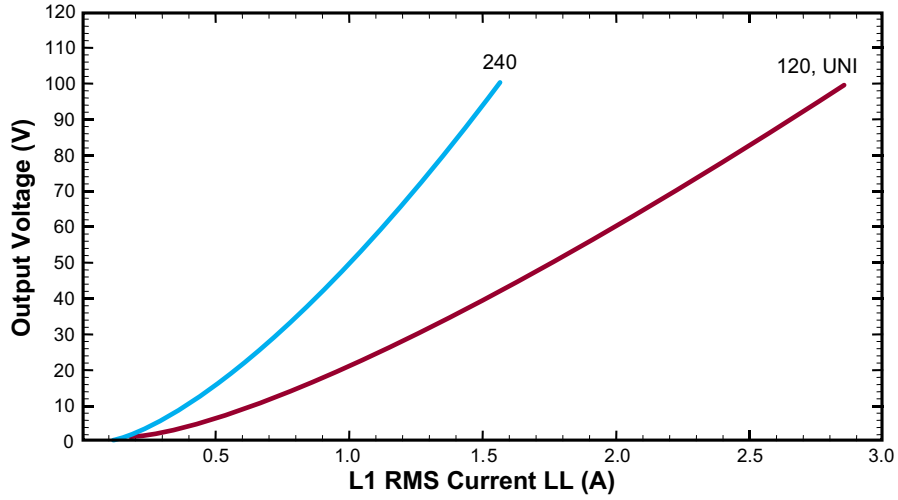


Fig. 6 - L2 Inductance (µH) vs Output Voltage (V)

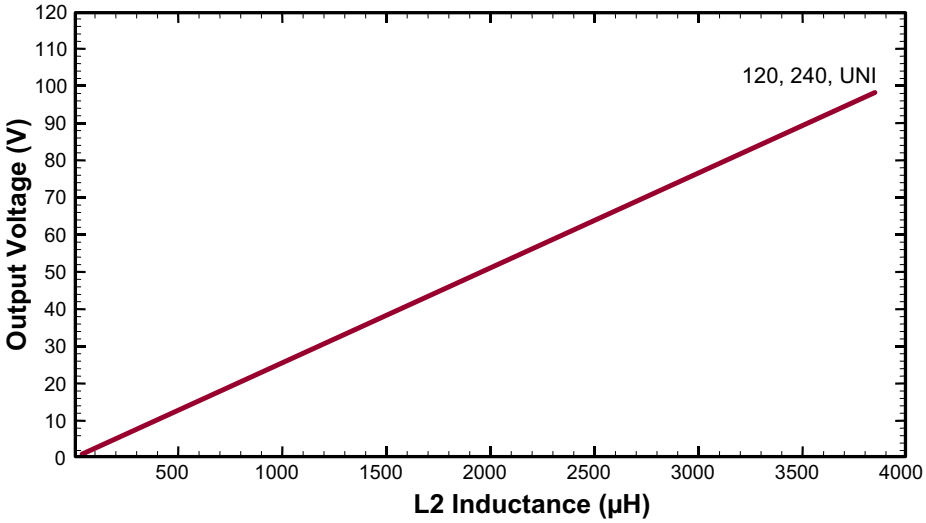


Fig. 7 - L2 Peak Current (A) vs Output Voltage (V)

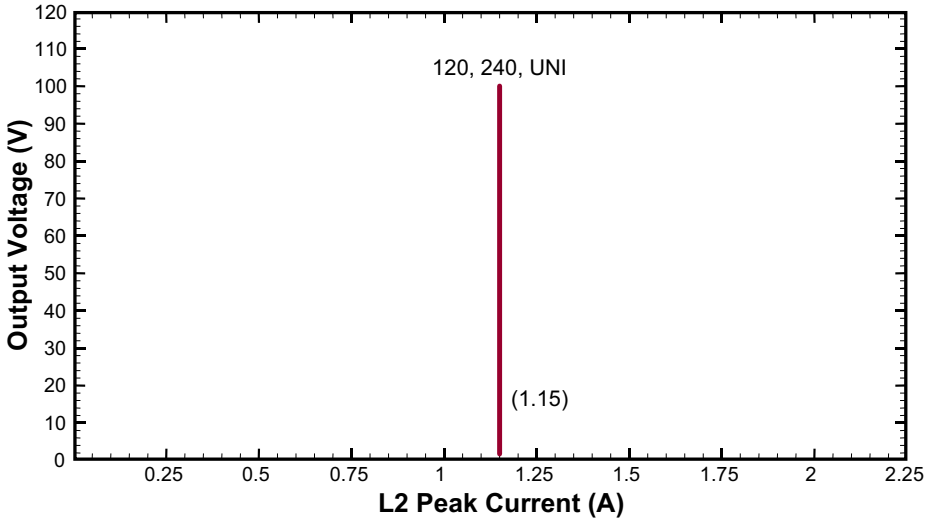


Fig. 8 - L2 RMS Current (A) vs Output Voltage (V)

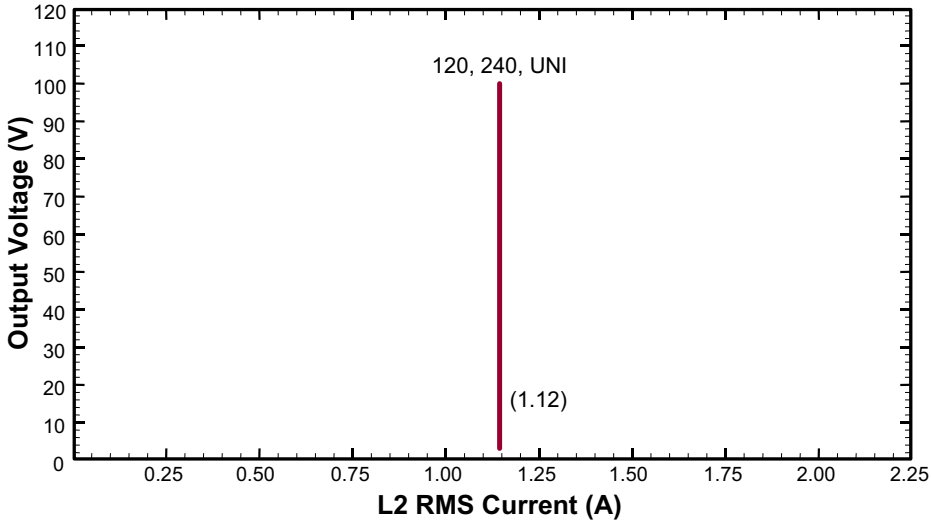


Fig. 9 - C1 Capacitance (µF) vs Output Voltage (V)

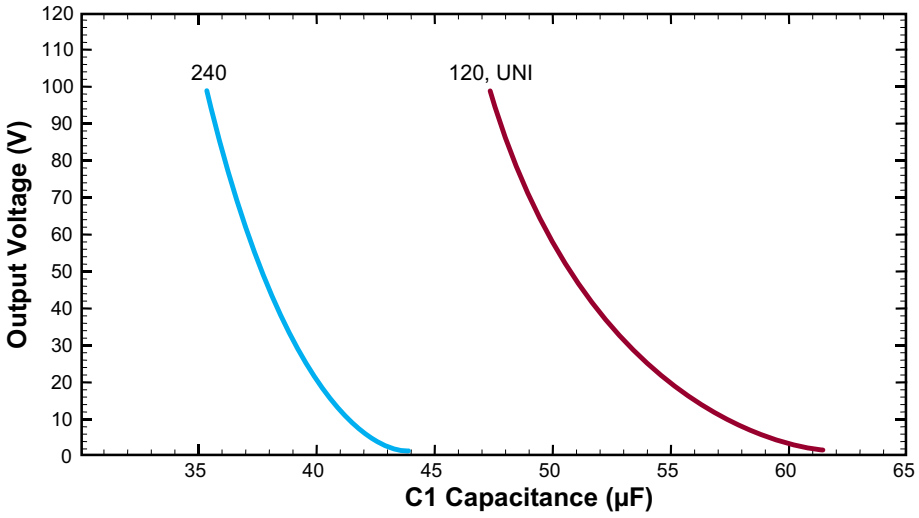


Fig. 10 - C1 RMS Current - LL (A) vs Output Voltage (V)

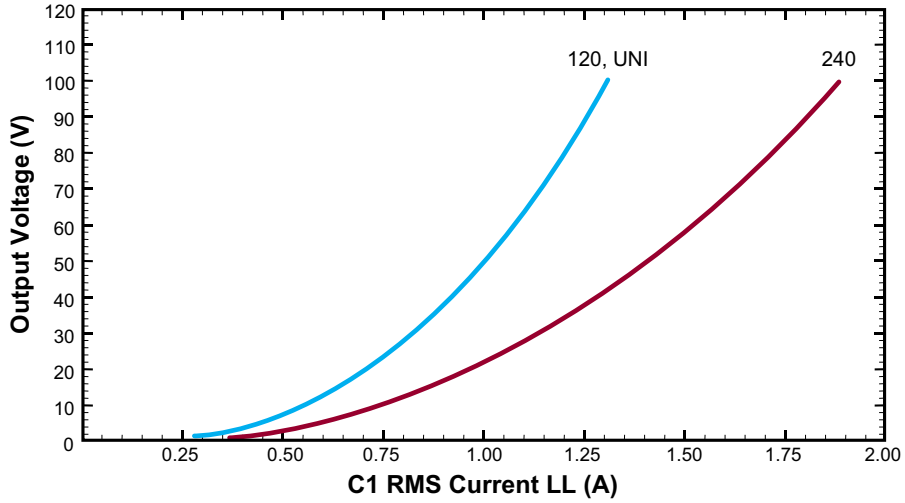


Fig. 11 - C1 Max Voltage - HL (V) vs Output Voltage (V)

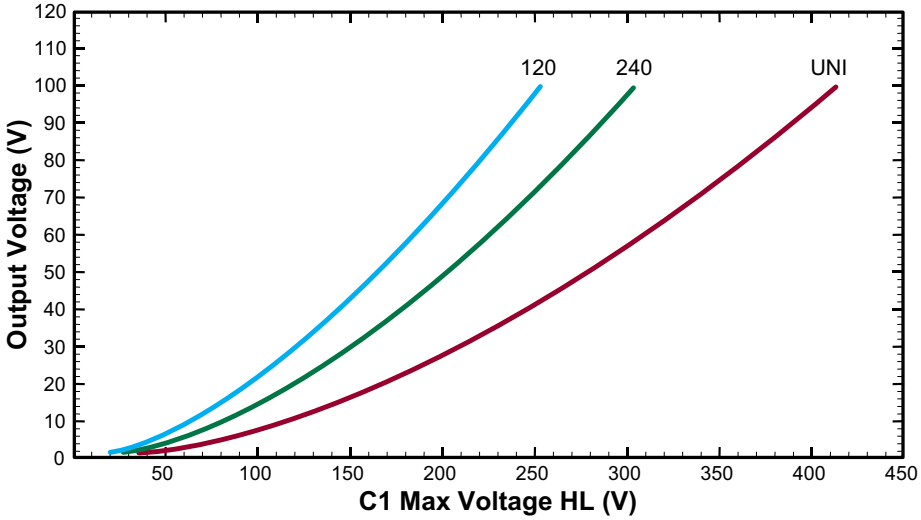


Fig. 12 - C1 Min Voltage - LL (V) vs Output Voltage (V)

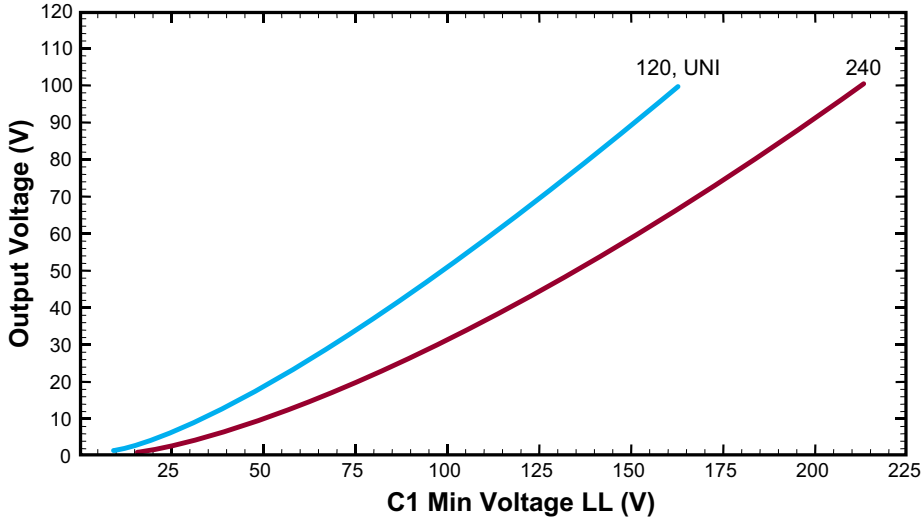


Fig. 13 - M1 Peak Current - LL (A) vs Output Voltage (V)

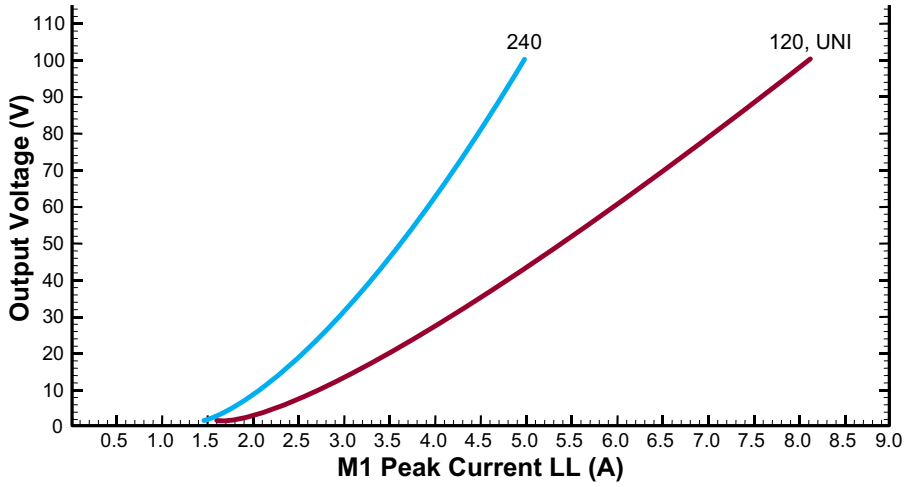


Fig. 14 - M1 Max RMS Current - LL (A) vs Output Voltage (V)

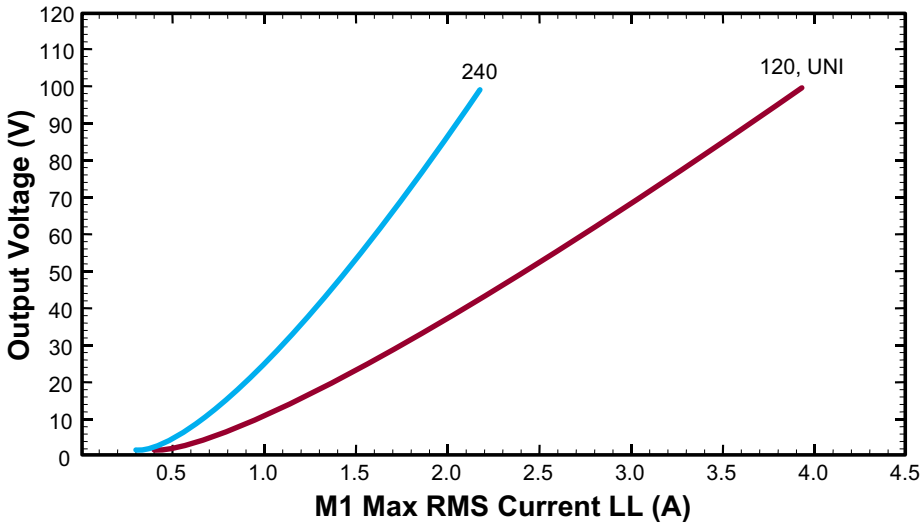


Fig. 15 - M1 Peak Drain Voltage - HL (V) vs Output Voltage (V)

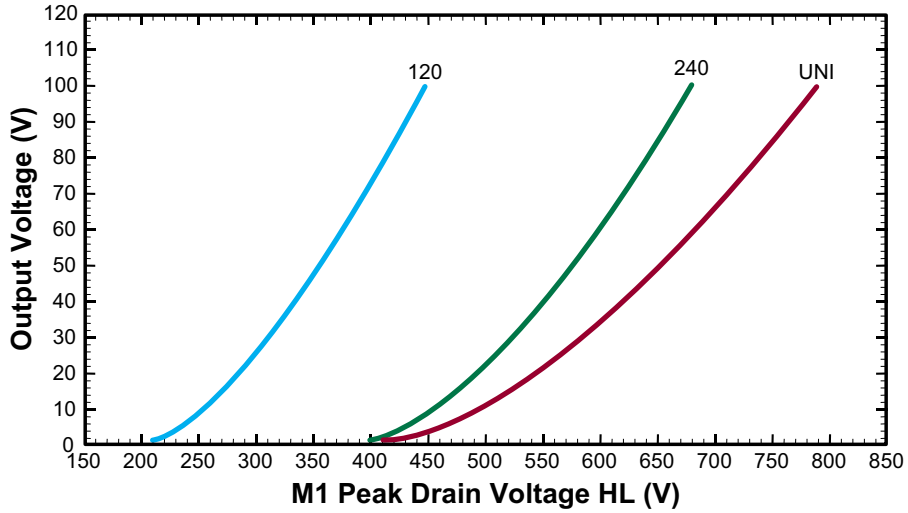


Fig. 16 - D1 Ave Forward Current - LL (A) vs Output Voltage (V)

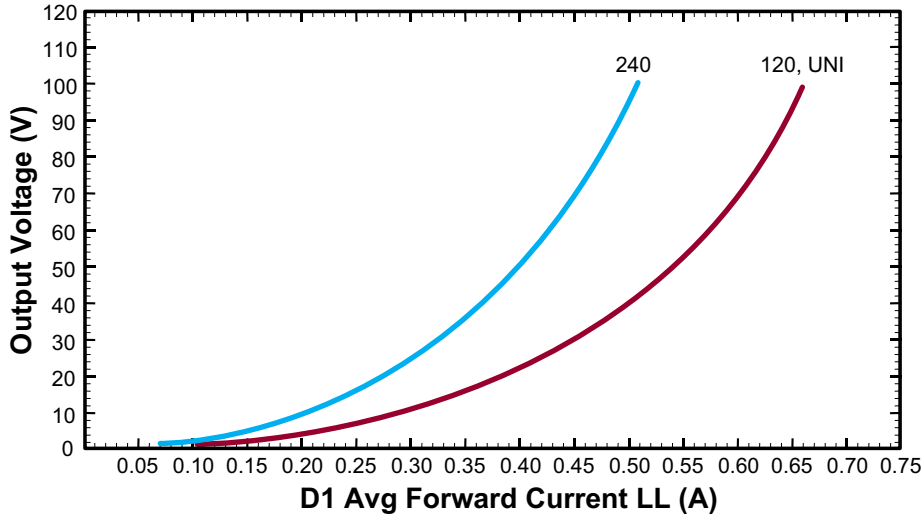


Fig. 17 - D1 Max Reverse Voltage - HL (V) vs Output Voltage (V)

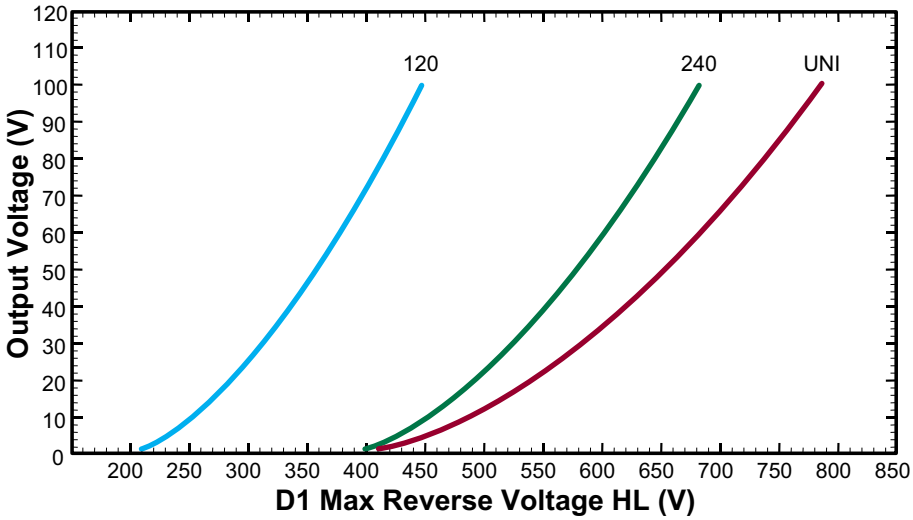


Fig. 18 - D2 Ave Forward Current - LL (A) vs Output Voltage (V)

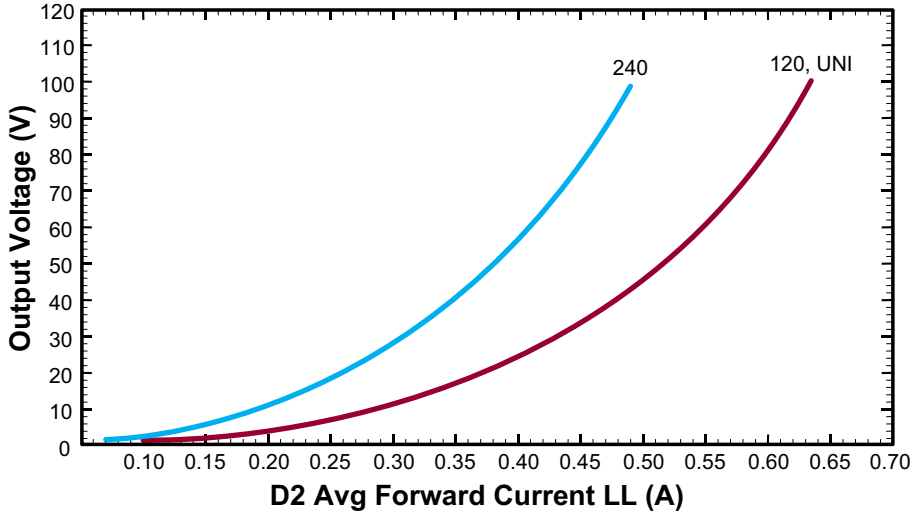


Fig. 19 - D2 Max Reverse Voltage - HL (V) vs Output Voltage (V)

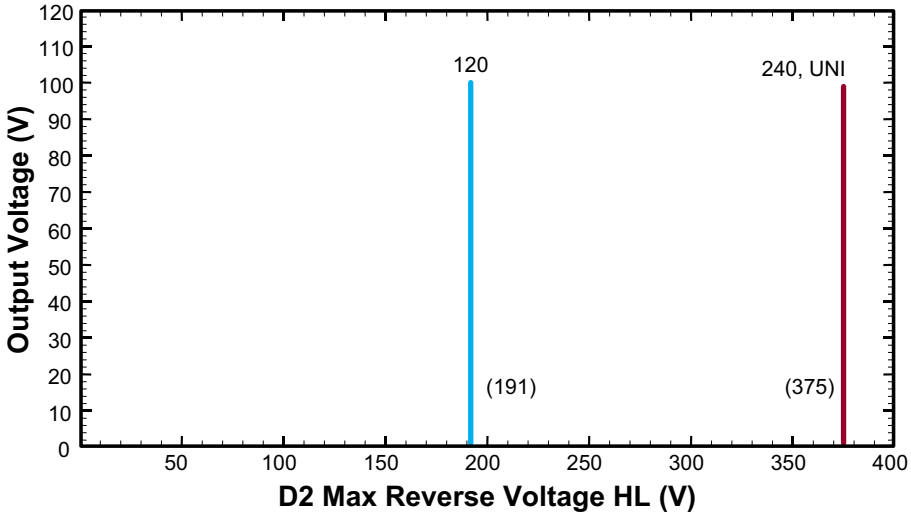


Fig. 20 - D3 Ave Forward Current - HL (A) vs Output Voltage (V)

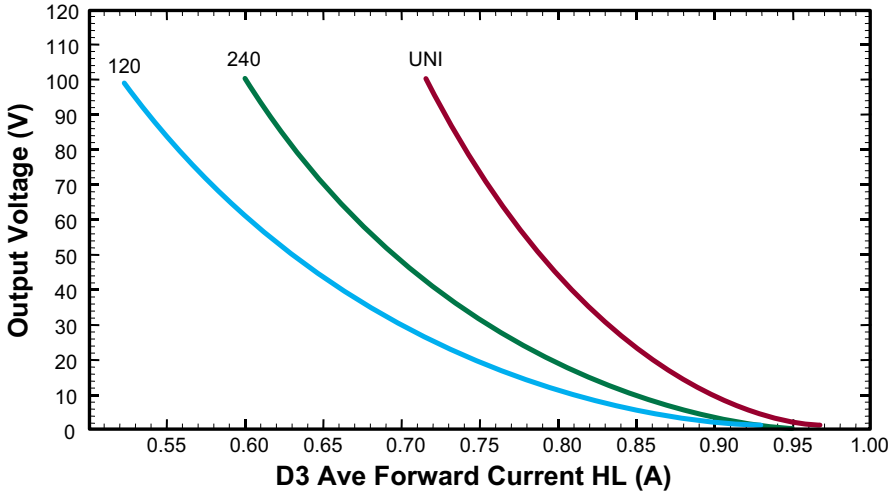


Fig. 21 - D3 Max Reverse Voltage - HL (V) vs Output Voltage (V)

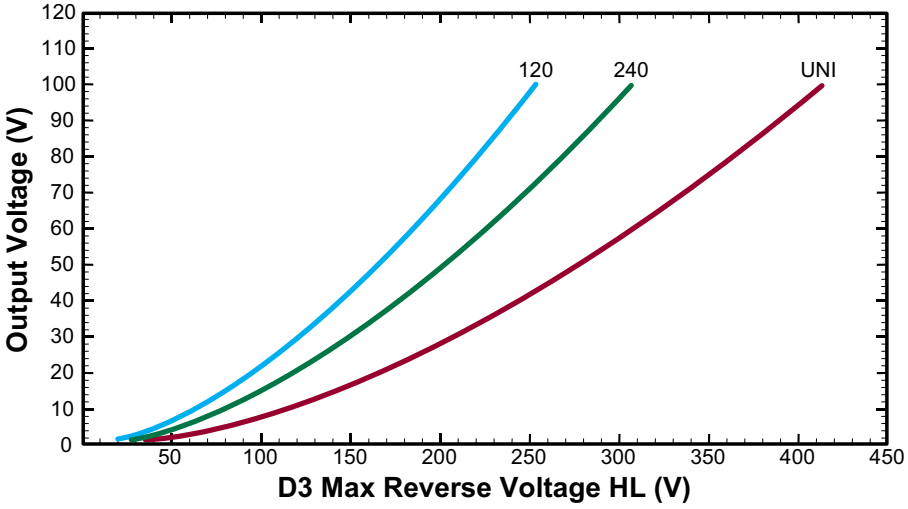


Fig. 22 - D4 Ave Forward Current - LL (A) vs Output Voltage (V)

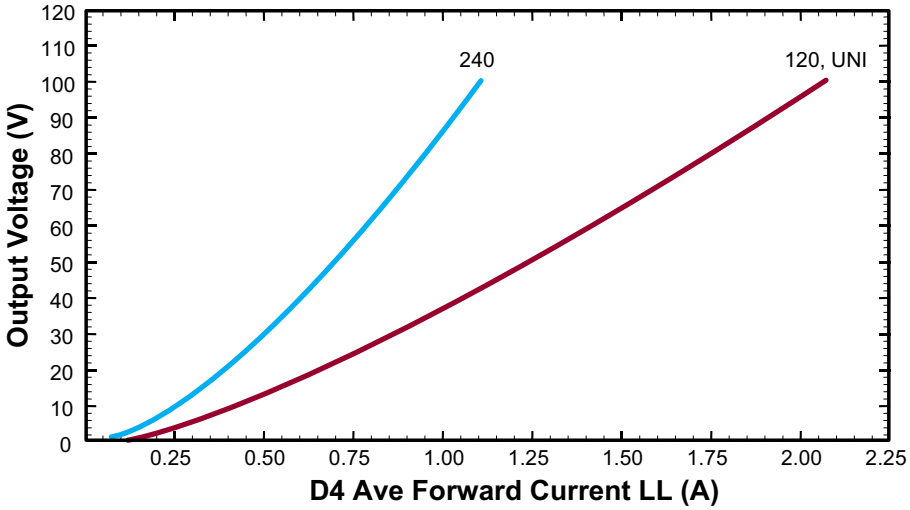


Fig. 23 - RS1, RS2: Resistance (mΩ) vs Output Voltage (V)

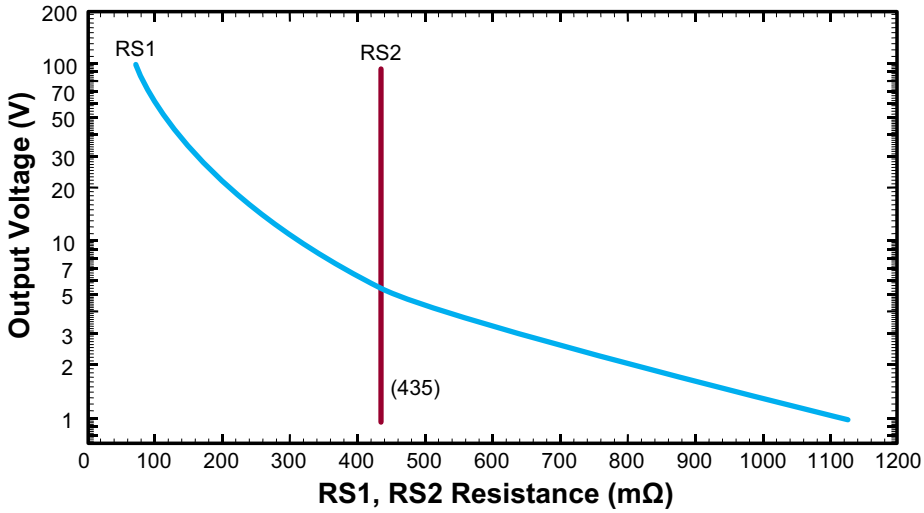


Fig. 24 - RS1, RS2: Power Dissipation - LL (mW) vs Output Voltage (V)

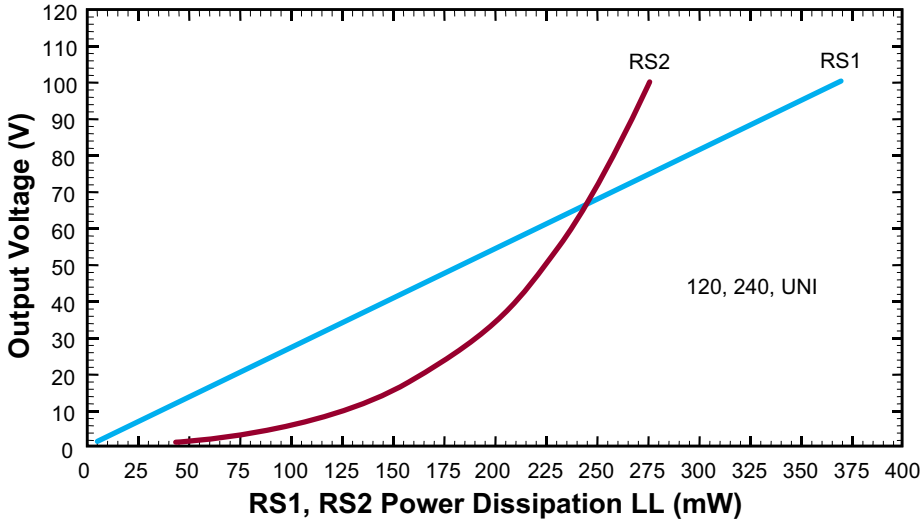


Fig. 25 - RCS1, RCS2: Resistance (kΩ) vs Output Voltage (V)

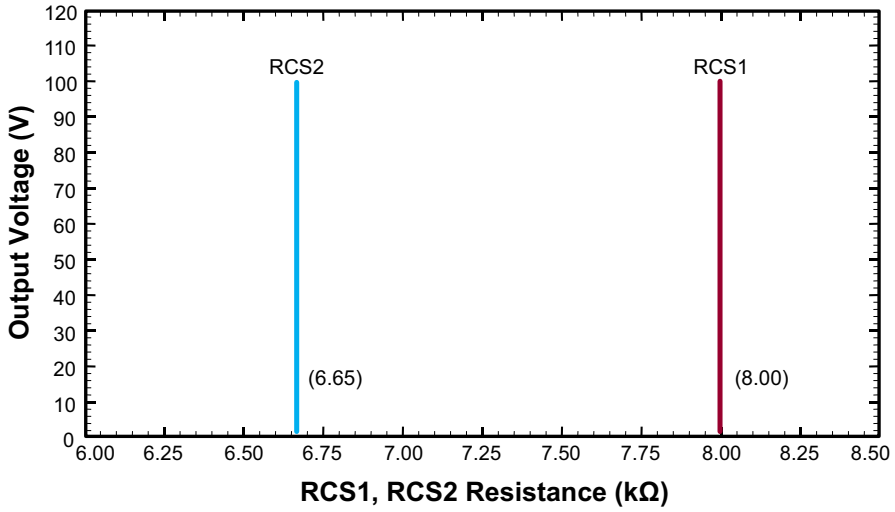


Fig. 26 - RT Resistance (kΩ) vs Output Voltage (V)

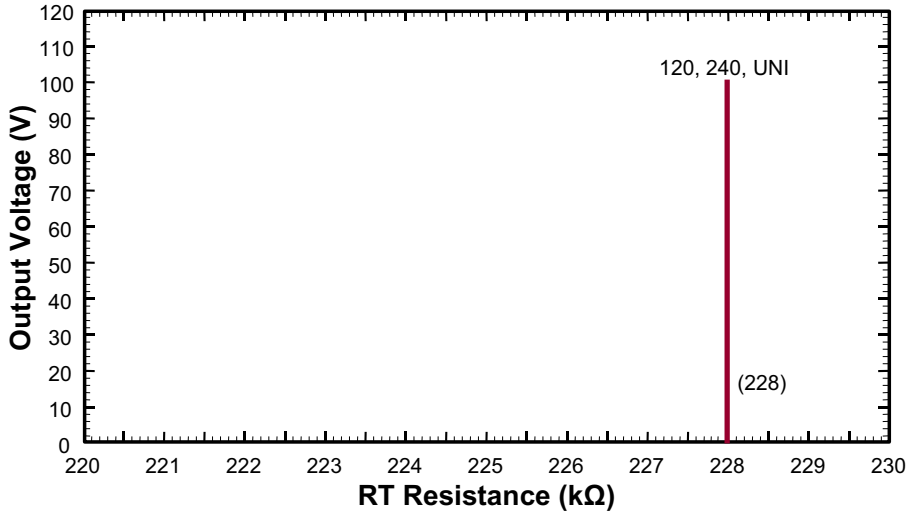


Fig. 27 - Min Duty Cycle - HL (%) vs Output Voltage (V)

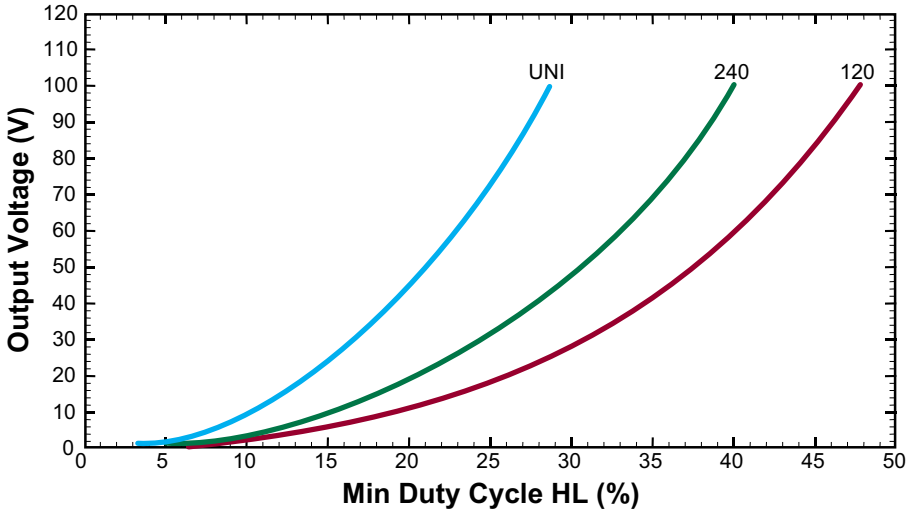


Fig. 28 - Max Duty Cycle - LL (%) vs Output Voltage (V)

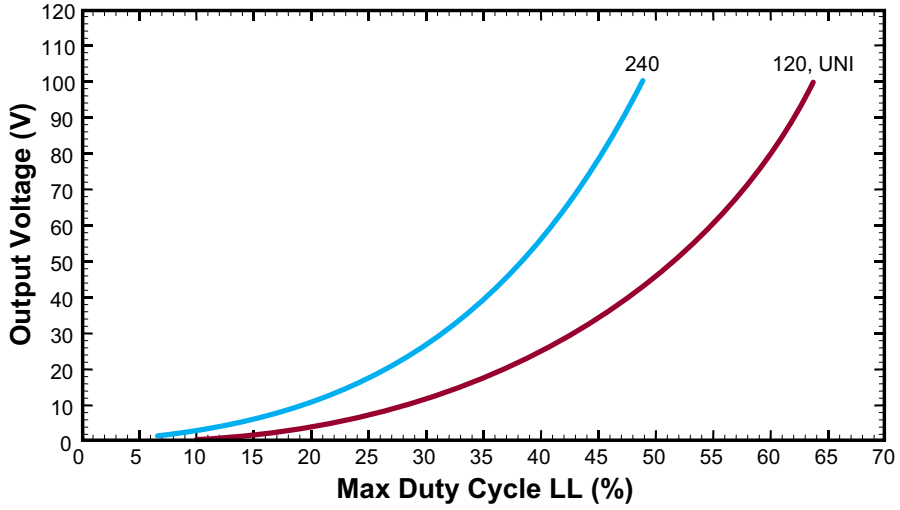


Fig. 29 - Min Switching Frequency - LL (kHz) vs Output Voltage (V)

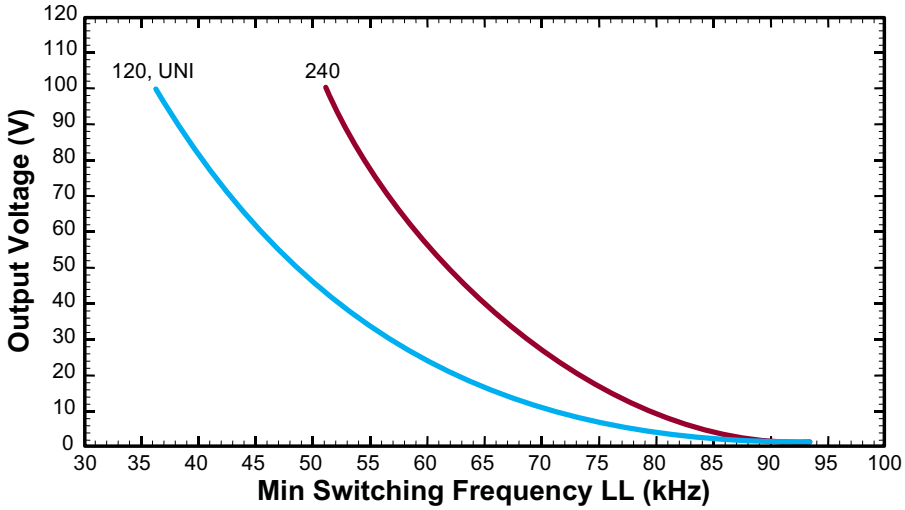
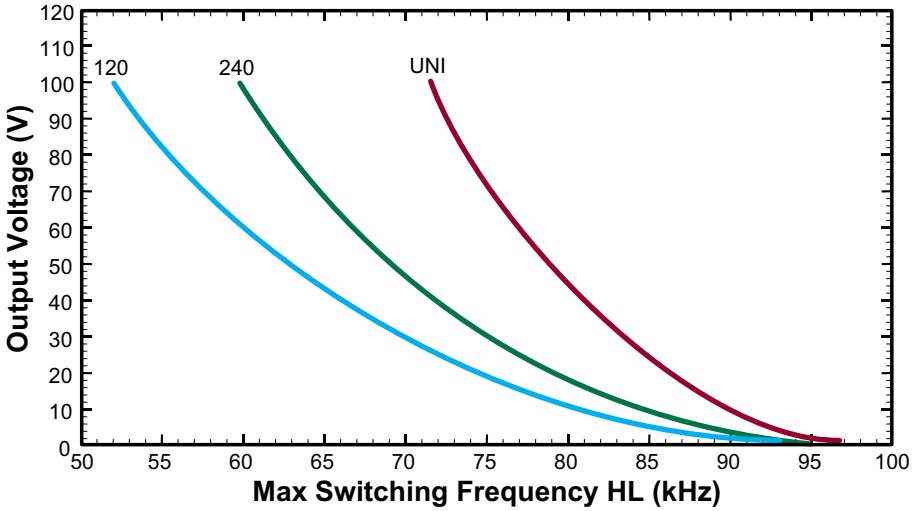


Fig. 30 - Max Switching Frequency - HL (kHz) vs Output Voltage (V)



Design Worksheet

Item	Parameter	Fig	AC Line	Base Design		I_O	T_{OFF}	Target Design		Units
				120V 24V		*0.50*	*1.5*	*0.5A 15µs*		
AC Line	P	1	-	*31.8*		M	✓	*15.9*		W
	Max RMS I	2	LL	*0.35*		M	✓	*0.18*		A
L1	L	3	-	*300*		D	M	*954*		µH
	Peak I	4	LL	*2.58*		M	✓	*1.29*		A
	RMS I	5	LL	*1.05*		M	✓	*0.52*		A
L2	L	6	-	*915*		D	M	*2745*		µH
	Peak I	7	-	*1.15*		M	✓	*0.575*		A
	RMS I	8	-	*1.12*		M	✓	*0.56*		A
C1	C	9	-	*57.1*		M	✓	*28.55*		µF
	RMS I	10	LL	*1.02*		M	✓	*0.51*		A
	Max V	11	HL	*105*		✓	✓	*105*		V
	Min V	12	LL	*62*		✓	✓	*62*		V
M1	Peak ID	13	LL	*3.69*		M	✓	*1.85*		A
	RMS ID	14	LL	*1.5*		M	✓	*0.75*		A
	Peak VD	15	HL	*295*		✓	✓	*295*		V
D1	Ave I	16	LL	*0.41*		M	✓	*0.205*		A
	Peak VR	17	HL	*295*		✓	✓	*295*		V
D2	Ave I	18	LL	*0.38*		M	✓	*0.19*		A
	Peak VR	19	HL	*191*		✓	✓	*191*		V
D3	Ave I	20	HL	*0.72*		M	✓	*0.36*		A
	Peak VR	21	HL	*104*		✓	✓	*104*		V
D4	Ave IF	22	LL	*0.72*		M	✓	*0.36*		A
RS1	R	23	-	*188*		D	✓	*3.76*		mΩ
	P	24	LL	*89*		M	✓	*44.5*		mW
RS2	R	23	-	*435*		D	✓	*348*		mΩ
	P	24	-	*174*		M	✓	*87*		mW
RCS1	R	25	-	*8.00*		✓	✓	*8.00*		kΩ
RCS2	R	25	-	*6.65*		✓	✓	*6.65*		kΩ
Timing	RT	26	-	*228*		✓	M	*342*		kΩ
	Min D	27	HL	*31.5*		✓	✓	*31.5*		%
	Max D	28	LL	*39.9*		✓	✓	*39.9*		%
	Min FS	29	LL	*61.8*		✓	D	*41.2*		kHz
	Max FS	30	HL	*69.0*		✓	D	*46.0*		kHz

LL (Low Line), HL (High Line), Base I_O (1A), Base T_{OFF} (10µs), M (Multiply), D (Divide), ✓ (No Change)

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