Sequential Linear LED Driver

Features

- Minimal component count
  (base config: CL8800 + 6 resistors + diode bridge)
- No magnetics, no capacitors
- Up to 13W output
- >115Lm/W using efficient LEDs
- 90% typical electrical efficiency
- > 0.9 power factor
- < 10% THD line current
- Low conducted EMI w/o filters
- 80–90% LED utilization
- Phase dimmer compatible with an RC network

Applications

- Fluorescent tube retrofit
- Incandescent & CFL bulb replacement
- General LED lighting

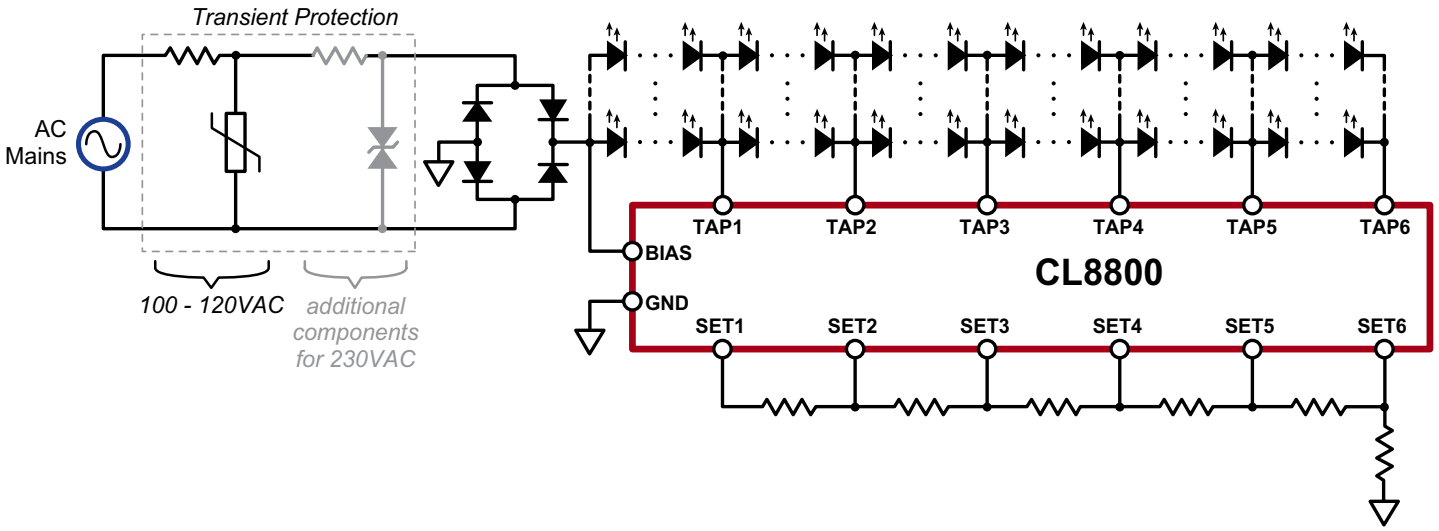
General Description

The CL8800 is designed to drive a long string of inexpensive, low current LEDs directly from the AC mains. A basic driver circuit consists of the CL8800, six resistors, and a bridge rectifier. Two to four additional components are optional for various levels of transient protection. No capacitors, EMI filters, or power factor correction circuits are needed.

A string of series/parallel LEDs is tapped at six locations. Six linear current regulators sink current at each tap and are sequentially turned on and off, tracking the input sine wave voltage. Voltage across each regulator is minimized when conducting, providing high efficiency. Output current at each tap is individually resistor-adjustable. Cross-regulation, as the CL8800 switches from one regulator to another, provides smooth transitions. The current waveform can be tailored to optimize for input voltage range, line/load regulation, output power/current, efficiency, power factor, THD, dimmer compatibility, and LED utilization.

With the addition of an RC network, the driver is compatible with phase dimming.

Typical Application Circuit



Ordering Information

Part Number	Package Options	Packing
CL8800K6-G	40-Lead (6x6) QFN	490/Tray
CL8800K6-G M935	40-Lead (6x6) QFN	2000/Reel
CL8800K63-G	33-Lead (6x6) QFN*	490/Tray
CL8800K63-G M935	33-Lead (6x6) QFN*	2000/Reel

- G indicates package is RoHS compliant ('Green')
** Consult factory for package option availability*

ESD Sensitive Device

Absolute Maximum Ratings

Parameter	Value
V_{BIAS}, V_{TAP1}	–0.5V to +550V
V_{TAP2-6}	–0.5V to +320V
V_{SET1-6}	4.0V
Operating junction temperature	-40ºC to +125ºC
Storage temperature, T_S	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
40-Lead QFN	24°C/W
33-Lead QFN	24°C/W

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

40-Lead QFN (K6)

L = Lot Number
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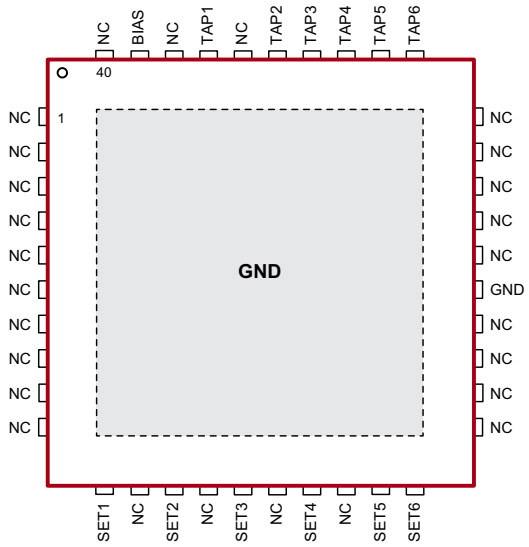
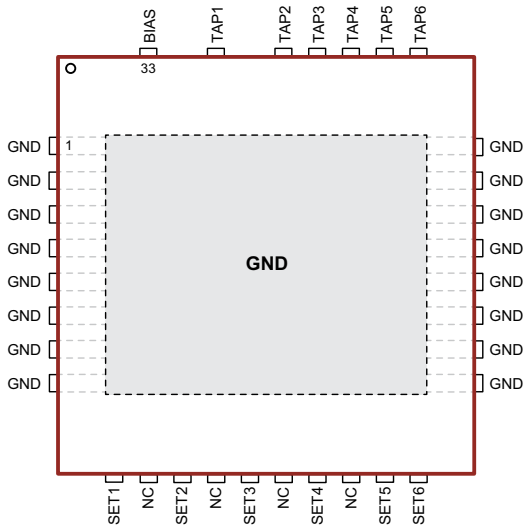
33-Lead QFN (K6)

Pin Configuration



40-Lead QFN (K6)
(top view)



33-Lead QFN (K6)
(top view)

Note:

The CL8800 will initially be offered in a 40-lead package and will switch to the 33-lead package when available. Printed circuit boards should be laid out for the 33-lead package.

Recommended Operating Conditions

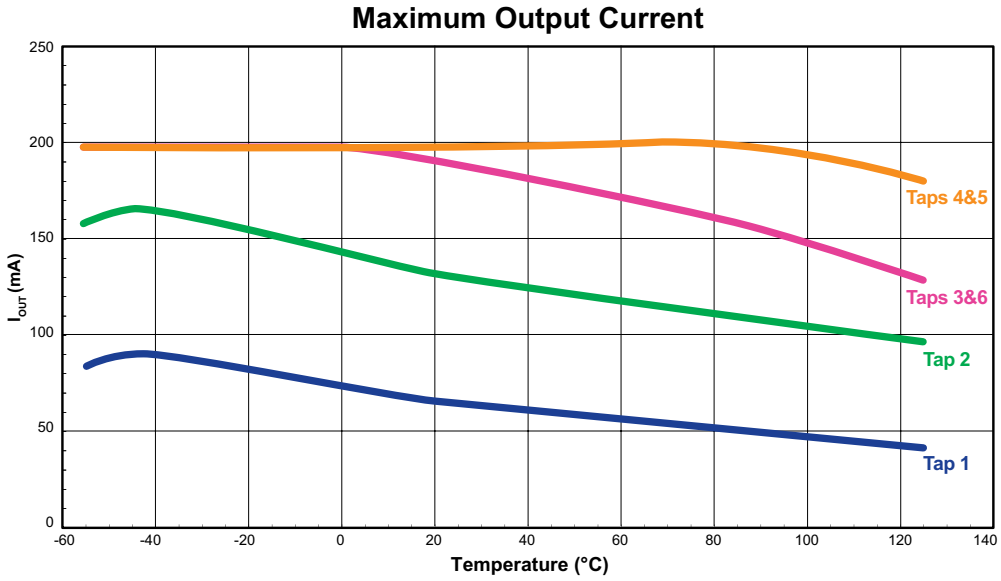
Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{OUT}	Output current	TAP1	-	-	40	mA	---
		TAP2	-	-	90		
		TAP3	-	-	115		
		TAP4	-	-	115		
		TAP5	-	-	115		
		TAP6	-	-	115		
V_{OUT}	Output voltage	TAP1	-	-	400	V	Non-conducting
		TAP2-6	-	-	300		Non-conducting
		TAP1-6	-	-	*(1)*		Conducting
V_{BIAS}	Applied BIAS voltage		-	-	440	V	---

Note:
(1) Voltage capability is determined by power dissipation (V × I).

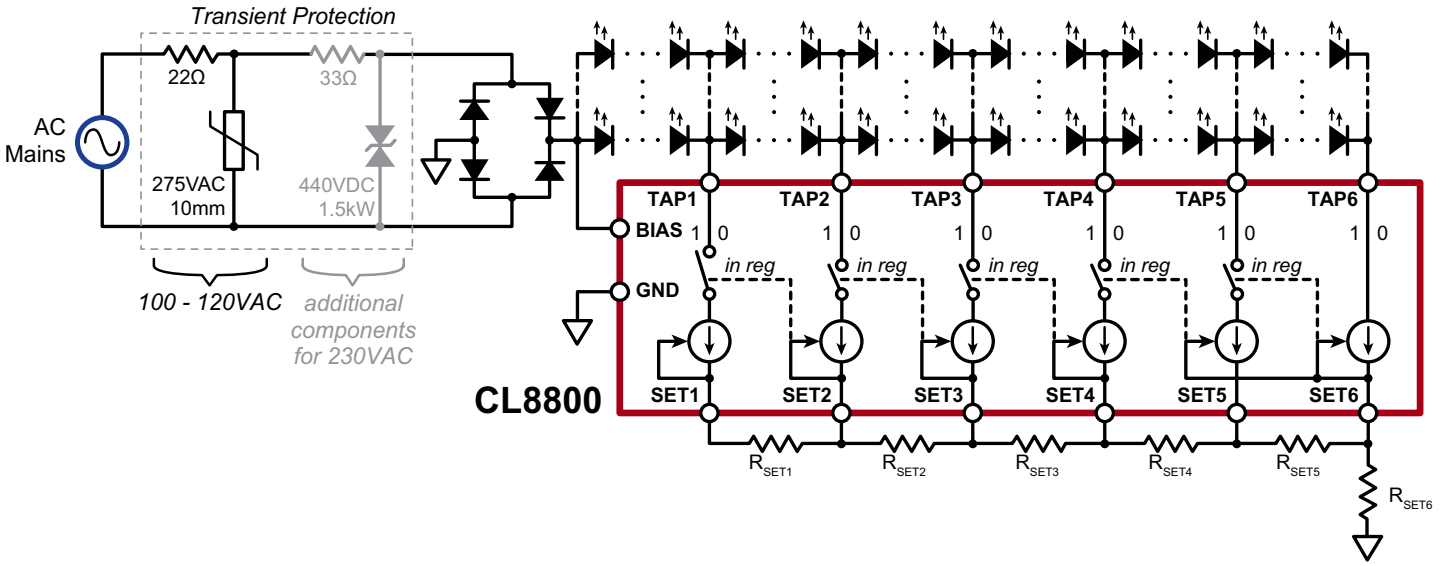
Electrical Characteristics *(over recommended operating conditions at 25°C unless specified otherwise)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{BIAS}	BIAS pin input current		-	250	410	µA	V_{BIAS} = 340V
$I_{TAP(ON)}$	Output current, on	TAP1	40	-	-	mA	V_{TAP1} = 30V, $V_{SET1\sim6}$ = GND
		TAP2	90	-	-		V_{TAP2} = 17V, $V_{SET1\sim6}$ = GND
		TAP3	115	-	-		V_{TAP3} = 17V, $V_{SET1\sim6}$ = GND
		TAP4	115	-	-		V_{TAP4} = 17V, $V_{SET1\sim6}$ = GND
		TAP5	115	-	-		V_{TAP5} = 17V, $V_{SET1\sim6}$ = GND
		TAP6	115	-	-		V_{TAP6} = 17V, $V_{SET1\sim6}$ = GND
$I_{TAP(OFF)}$	Output current, off		-	0	10	µA	TAP1 - 6, V_{BIAS} = 312V
V_{REG}	Regulation voltage at SET pins	SET1 - 5	1.80	2.00	2.20	V	---
		SET6	1.89	2.10	2.31		

Output Current Thermal Characteristics



Simplified Block Diagram



Overview

Designing a driver to meet particular requirements may be a difficult task considering the number of design variables (18): tap current (6), number of series-connected LEDs per segment (6), and the number of parallel-connected LEDs per segment (6). Manually selecting values will provide light, but the chosen values may be far from optimal in regards to efficiency, LED utilization, line regulation, etc.

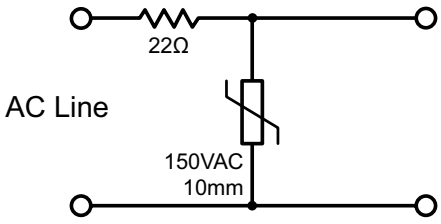
Contact your nearest Supertex Field Applications Engineer for design assistance. MathCAD and Excel worksheets are available by contacting *apps@supertex.com*.

In addition to configuring the driver, several circuits may be employed to increase reliability, performance, and cost. The following sections briefly describe these circuits.

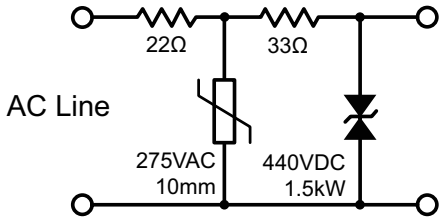
Transient Protection

Since the driver circuits have no need for capacitors that could otherwise absorb transient energy, nor is there a need for EMI filters that would block transients, the full burden of transient protection is borne by the protection circuit. The two-stage approach in the following schematics provide 2.5kV protection, both pulse and ring per EN 61000-4-5 and EN 61000-4-12, six hits each.

100 to 120VAC Transient Protection



230VAC Transient Protection



Zener Substitution

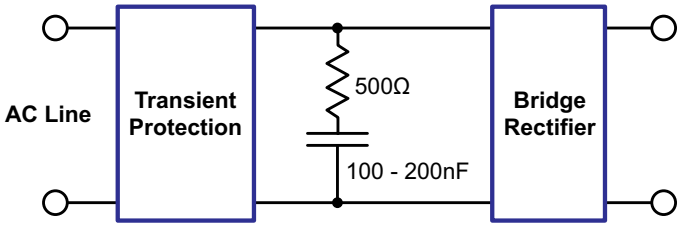
Zeners may be substituted for LEDs in the bottom stages. The last 1 or 2 stages contribute little to light output - they are mainly to off-load the adjacent upstream regulator at high line voltages to minimize losses. Zener substitution advantages include minimizing unlit LEDs at low line for better light uniformity, better line regulation at high line, fewer LEDs for lower cost and less PCB area, and fewer board-to-board connections. Disadvantages include slightly reduced efficiency at high line, and additional heat load on the driver board.

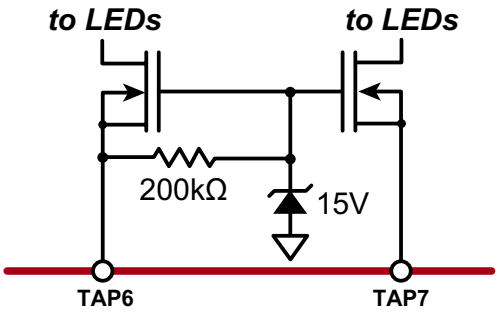
Phase Dimming

As with any light load, the LED lamp might not draw enough current to assure proper dimmer operation. This is especially true for 230VAC dimmers. Triacs used in dimmers require a minimum latching current when triggered to place the triac in the latched-on state. Once latched, a minimum holding current is required to maintain the triac in the on state. Latching current is many times greater than the holding current, and is the main concern with dimmer compatibility.

Higher latching current can be provided by a simple series RC network across the AC line. A short time constant provides a current spike at the turn-on edge.

Less common is inadequate holding current. The minimum dimming holding current is typically 10-20mA. Tap1 at 40mA (max) exceeds the minimum.





Power Boost

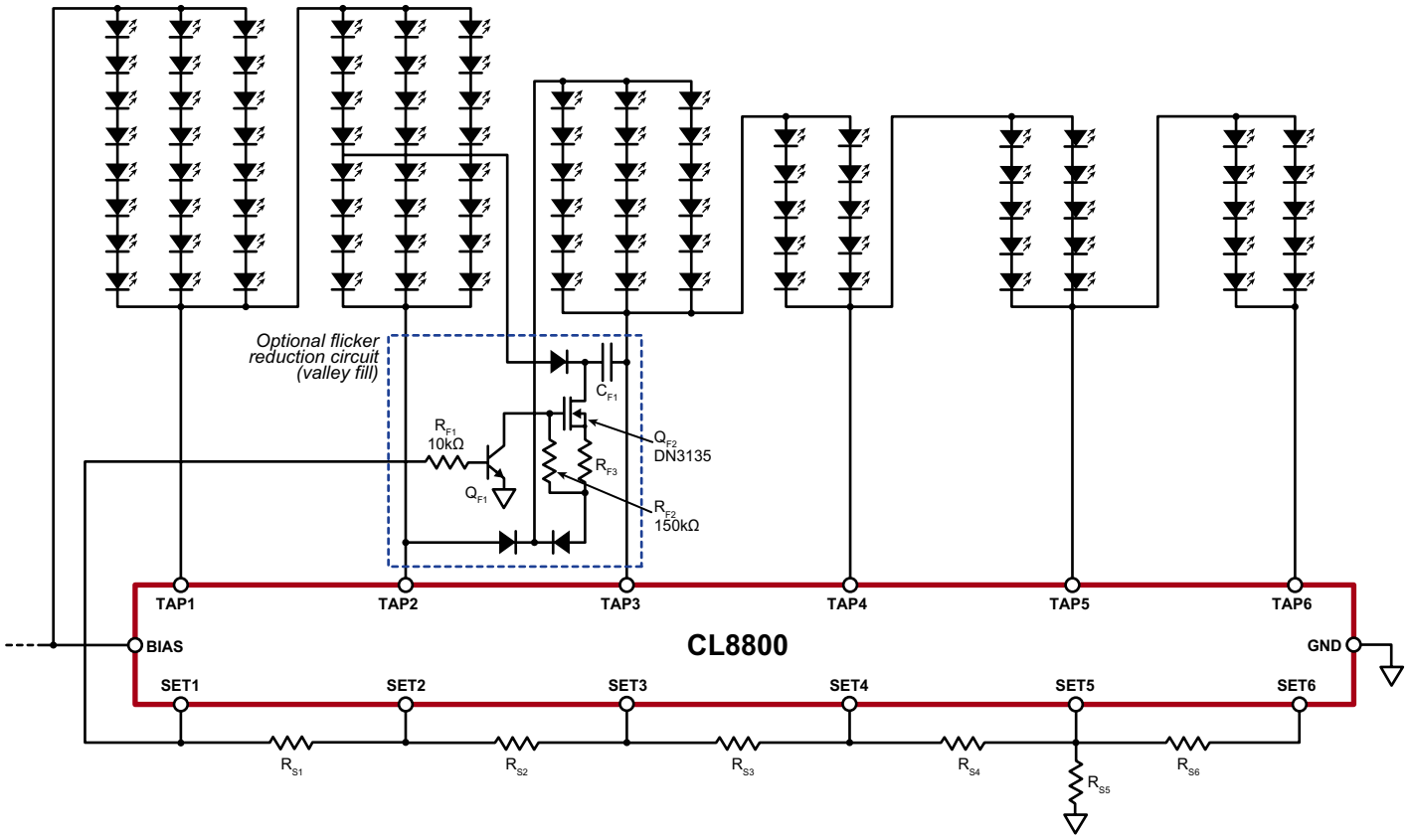
Higher output power can be achieved by off-loading a portion of the power dissipation from the CL8800 to external FETs. The circuit below drops most of the tap voltage across the FETs, thereby shifting the bulk of the dissipation to the FET.

Flicker

Twice per AC line cycle the line voltage crosses zero volts, during which time there is no light output.

The circuit below can provide 5-10% valley fill. It has little effect on input current waveshape (THD, PF) and efficiency.

Valley Fill Circuit



Pin Description (40-Lead K6)

Pin #	Pin Name	Description
1 - 10	NC	No internal connection (use for heat sink ground plane pass through).
11	SET1	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
12	NC	No internal connection.
13	SET2	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
14	NC	No internal connection.
15	SET3	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
16	NC	No internal connection.
17	SET4	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
18	NC	No internal connection.
19	SET5	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
20	SET6	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
21 - 24	NC	No internal connection (use for heat sink ground plane pass through).
25	GND	Circuit common. Connect to bridge rectifier return (use for heat sink ground plane pass through).
26 - 30	NC	No internal connection (use for heat sink ground plane pass through).
31	TAP6	Current regulator outputs. Connect to taps along the LED string.
32	TAP5	
33	TAP4	
34	TAP3	
35	TAP2	
36	NC	No internal connection.
37	TAP1	Current regulator outputs. Connect to taps along the LED string.
38	NC	No internal connection.
39	BIAS	Provides bias for driver. Connect to rectified AC.
40	NC	No internal connection.
Underside plate (GND)		For heatsinking purposes, it should be soldered to a 4.0cm^2 exposed copper area. It should also be electrically connected to circuit common (GND).

Note:

The high voltage pins are located on one side of the package and are arranged from lowest voltage to highest. Pin-to-pin voltage gradients are minimized.

Pin Description (33-Lead K6)

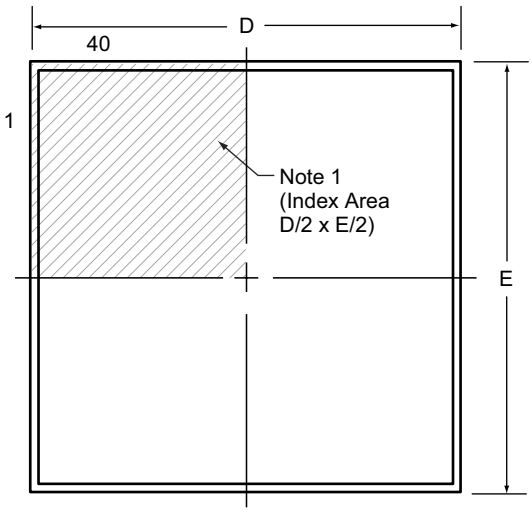
Pin #	Pin Name	Description
1 - 8	GND	Circuit common (use for heat sink ground plane pass through).
9	SET1	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
10	NC	No internal connection.
11	SET2	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
12	NC	No internal connection.
13	SET3	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
14	NC	No internal connection.
15	SET4	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
16	NC	No internal connection.
17	SET5	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
18	SET6	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
19 - 20	GND	Circuit common (use for heat sink ground plane pass through).
21	GND	Circuit common. Connect to bridge rectifier return (use for heat sink ground plane pass through).
22 - 26	GND	Circuit common (use for heat sink ground plane pass through).
27	TAP6	Current regulator outputs. Connect to taps along the LED string.
28	TAP5	
29	TAP4	
30	TAP3	
31	TAP2	
32	TAP1	
33	BIAS	Provides bias for driver. Connect to rectified AC.
Underside plate (GND)		For heatsinking purposes, it should be soldered to a 4.0cm^2 exposed copper area. It should also be electrically connected to circuit common (GND).

Note:

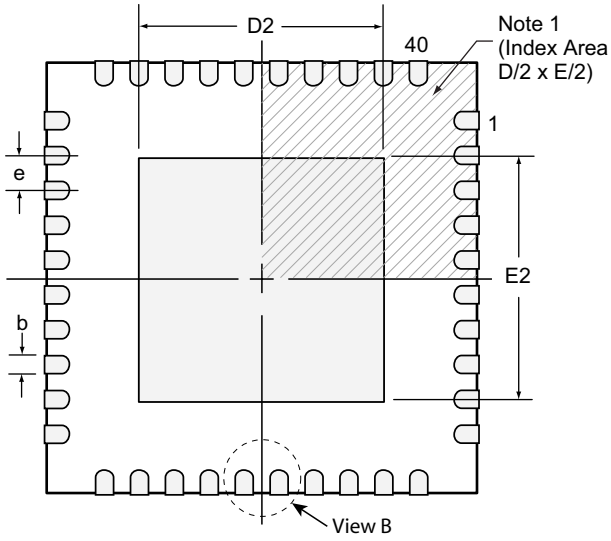
The high voltage pins are located on one side of the package and are arranged from lowest voltage to highest. Pin-to-pin voltage gradients are minimized.

40-Lead QFN Package Outline (K6)

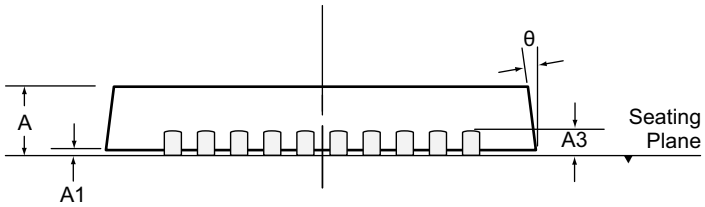
6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



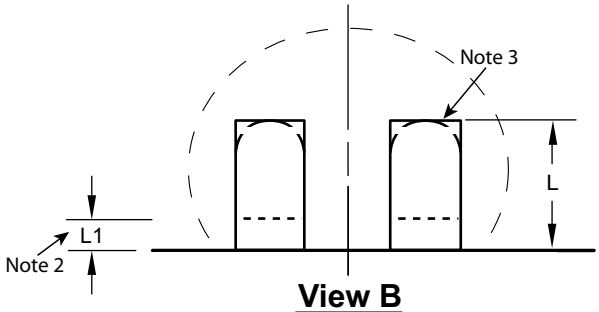
Top View



Bottom View



Side View



View B

Notes:

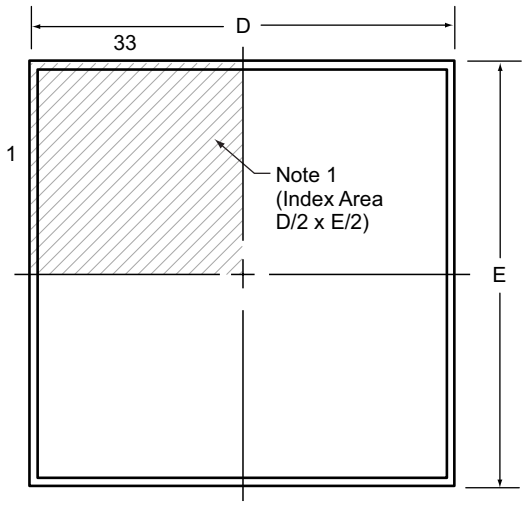
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

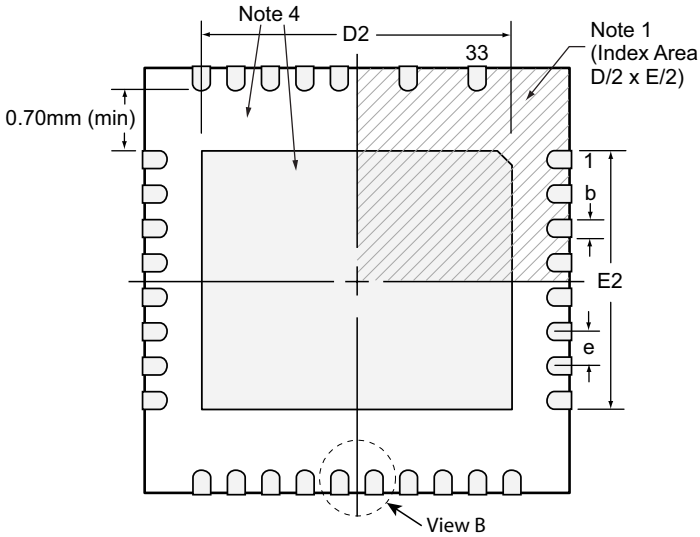
JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-40QFNK66X6P050, Version C041009.*

33-Lead QFN Package Outline (K6)

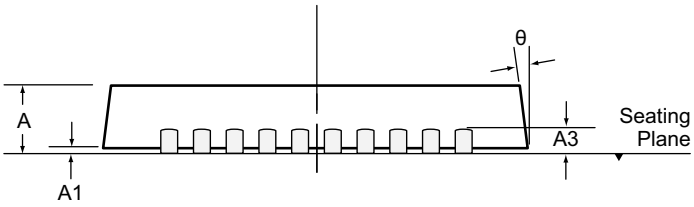
6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



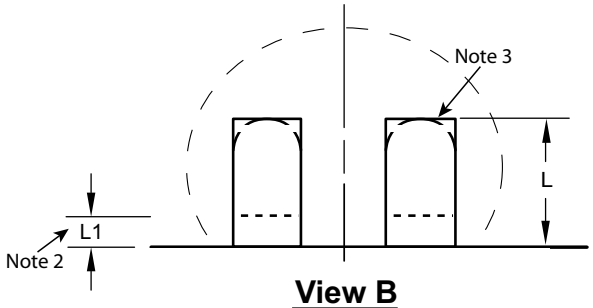
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*
4. *There will be an exposed DAP. A minimum of 0.7mm spacing will be maintained between the leads and the DAP.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85	4.00	5.85	3.60	0.50 BSC	0.30	0.00	0
	NOM	0.90	0.02		0.25	6.00	4.15	6.00	3.75		0.40	-	-
	MAX	1.00	0.05		0.30	6.15	4.25	6.15	3.85		0.50	0.15	14

Drawings not to scale.
Supertex Doc. #: *DSPD-33QFNK636X6P050, Version A021312.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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