Boost Converter LED Drivers Using the Supertex HV9911

Introduction

Boost converters (Fig. 1.1) are ideal for LED driver applications where the LED string voltage is greater than the input voltage.

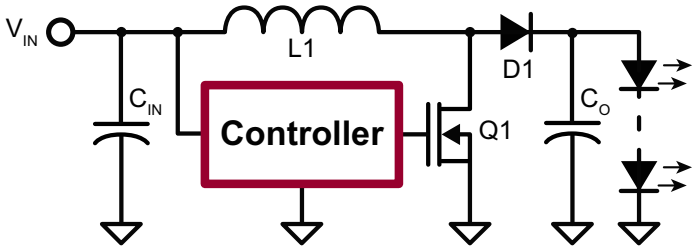


Fig. 1.1: Boost Converter LED Driver

- The converter can easily be designed to operate at efficiencies greater than 90%.
- Both the source of the FET and LED string are connected to a common ground. This simplifies sensing of the LED current (unlike the buck converter where we have to choose between either a high side FET driver or a high side current sensor).
- The input current is continuous which makes it easy to filter the input ripple current (and easier to meet any required conducted EMI standards).
- Failure of the switching FET will not damage the LEDs.

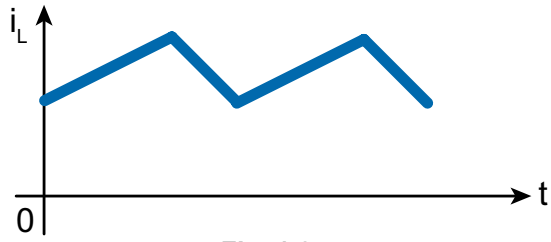


Fig. 1.2a:
Inductor Current for CCM Boost

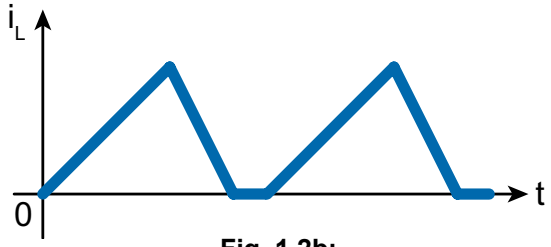


Fig. 1.2b:
Inductor Current for DCM Boost

However, boost converters have some disadvantages, especially when used as LED drivers (due to the low dynamic impedance of the LED string).

- The output current of the boost converter is a pulsed waveform. Thus, a large output capacitor is required to reduce the current ripple in the LED current.
- The large output capacitor makes PWM dimming more challenging as turning the boost converter on and off to achieve PWM dimming means the capacitor will have to be charged and discharged every PWM dimming cycle. This increases the rise and fall times of the LED current.
- Peak current control of the boost converter to control the LED current (as in the case of a HV9910 based buck control) is not possible. Closed loop is required to stabilize the converter. This also complicates PWM dimming, as the controller will need to have a large bandwidth to achieve the required response times.
- There is no control over the output current during output short circuit conditions, as turning off the switching FET will have no effect on the short circuit current. Also, if any input voltage transient causes the input voltage to increase to a value greater then the LED string voltage, there will be a surge of current into the LEDs which might damage them.

The boost converter can be operated in two modes – either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). The mode of operation of the boost converter is determined by the waveform of the inductor current. Fig. 1.2a is the inductor current waveform for a CCM boost converter whereas Fig.1.2b is the inductor current waveform for a DCM boost converter.

The CCM boost converter is used when the maximum step-up ratio (ratio of output voltage to input voltage) is less than or equal to 6 and at input current levels more than 1.0A. If larger boost ratios are required, the DCM boost converter is used. However, in the discontinuous conduction mode, the currents have large peak values, increasing the core losses in the inductor as well as increased rms current values. Thus, the DCM boost converters are typically less efficient than the CCM boost converters and are limited to lower power levels.

Supertex's HV9911 IC is a closed loop, peak current controlled, switch-mode converter LED driver, which has built-in features to overcome the disadvantages of the boost converter. The IC includes a 9.0 - 250V input voltage regulator which would enable the IC to work from the input voltage of the boost converter without the need for an external power supply for the IC. It includes a 2% accurate reference (over temperature) which enables a highly accurate LED current control. The IC also features a disconnect FET driver which can be used to disconnect the LED string during output short circuit or input over-voltage conditions. This disconnect FET is also used by the HV9911 to dramatically improve the PWM dimming response of the converter (see PWM Dimming Section).

Section I of this application note will describe the features of the HV9911 and explain how the features help overcome the shortcomings of the boost converter, Section II discusses a design example for a CCM boost LED driver, and Section III discusses an example for a DCM boost LED driver using the HV9911.

Section I – HV9911

The internal structure of the HV9911 is shown in Fig. 1.3.

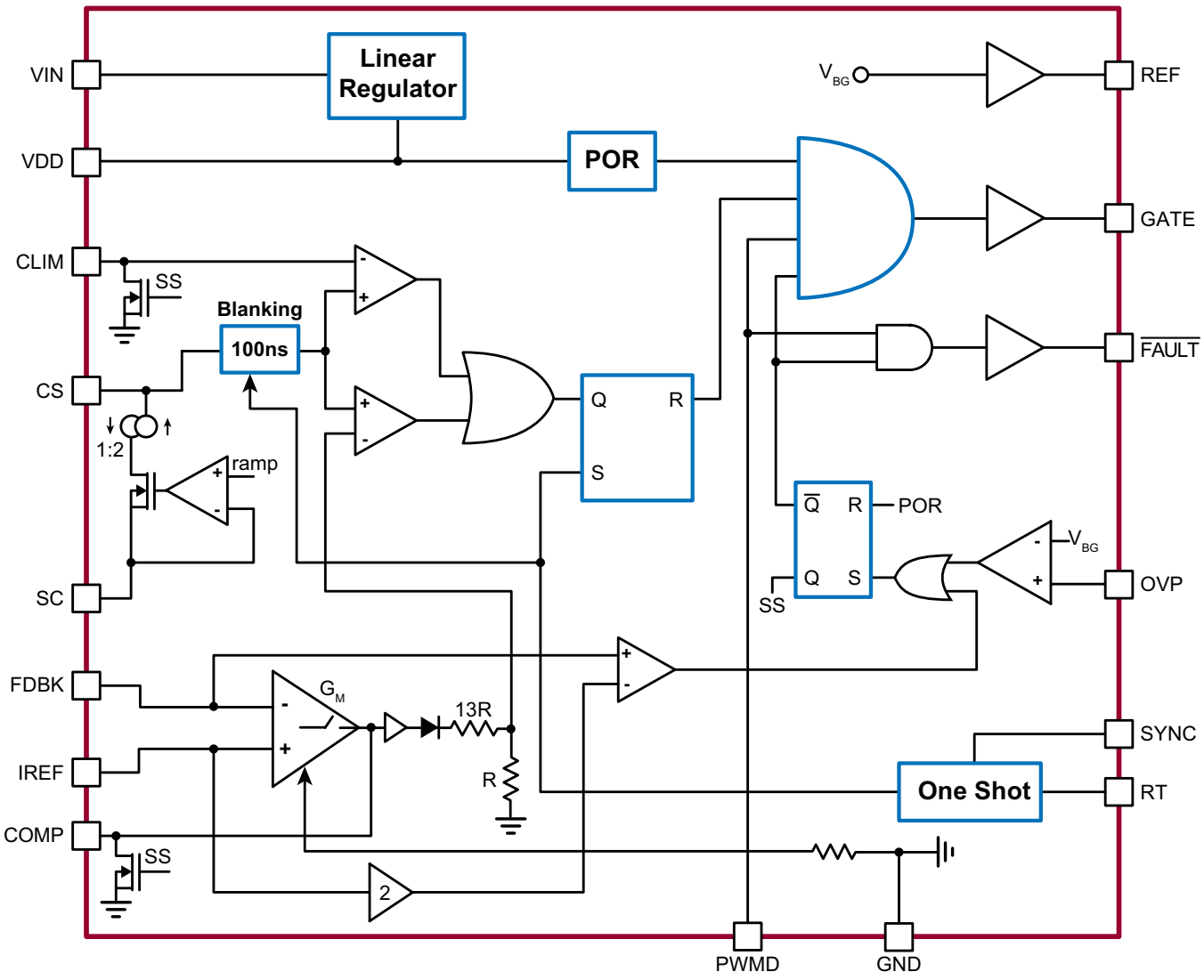


Fig. 1.3: Internal Circuit of the HV9911

The internal high voltage regulator provides a regulated 7.75V from a 9.0 - 250V input, which is used to power the IC. To increase the input voltage range of the IC, a 200V, 2.0W Zener diode can be placed between the input voltage and the VIN pin of the IC (Fig. 1.4). This would increase the input voltage range to about 450VDC. This would also help to divert the power dissipation away from the IC and into the Zener diode.

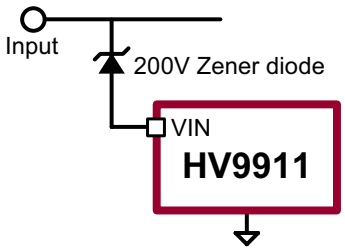


Fig. 1.4: Increasing the Input Voltage Rating

The VDD pin of the IC can be overdriven (if necessary) with an external voltage source through a diode. The diode will help to prevent damage to the HV9911 if the external voltage becomes less than the internally regulated voltage. The maximum steady state voltage that can be applied to the HV9911 is 12V (with a transient voltage rating of 13.5V). Thus an 11V ± 5% power supply would be ideal to overdrive the HV9911.

The HV9911 includes a buffered 1.25V, 2% accurate reference voltage. This reference can be used to set the current reference level as well as the input current limit level. This reference is also used internally to set the over voltage set point.

The oscillator of the HV9911 can be set by using an external resistor. If the resistor is connected between the RT and GND pins, the converter operates in a constant frequency mode, whereas if it is connected between the RT and GATE pins, the converter operates in a constant off-time mode (slope compensation is not necessary to stabilize the converter operating in a constant off-time). In both cases, the time (time period or off-time) can be set to any value between 2.8 and 40µs using the equation given in the datasheet.

In the fixed frequency mode, multiple HV9911 ICs can be synchronized to a single switching frequency by connecting the SYNC pins of all the IC together. In a few cases, a large resistor (>300kΩ) might be needed from SYNC to GND to damp the ringing due to parasitic capacitances. When multiple HV9911s are synchronized together, it is recommended that the same resistor (corresponding to the nominal switching frequency) be connected at the RT pins of each HV9911.

Closed loop control is achieved by connecting the output current sense signal to the FDBK pin and the current reference signal to the IREF pin. The compensation network is connected to the COMP pin (output of the transconductance opamp) as shown in Fig. 1.5. The output of the amplifier is controlled by the PWM dimming signal. When the PWM dimming signal is high the output of the amplifier is connected to the compensation network and when the PWM dimming signal is low, the compensation network is disconnected from the amplifier. Thus, the capacitor(s) in the compensation network hold the voltage and when the PWM dimming signal goes high again, the compensation network is reconnected to the amplifier. This ensures that the converter starts at the correct operating point and a very good PWM dimming response is obtained without having to design a fast controller.

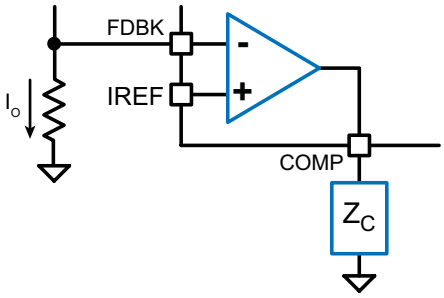


Fig. 1.5: Feedback Compensation

The $\overline{\text{FAULT}}$ pin is used to drive an external disconnect FET (Fig. 1-6). During the start-up of the HV9911, the $\overline{\text{FAULT}}$ pin is held low and once the IC starts-up the pin is pulled high. This connects the LEDs in the circuit and the boost converter powers up the LEDs. In case of an output over voltage condition or an output short circuit condition, an internal latch pulls the $\overline{\text{FAULT}}$ pin low and disconnects the LEDs. The $\overline{\text{FAULT}}$ pin is also controlled by the PWM dimming signal, so that the pin is high when the PWM dimming signal is high and vice-versa. This disconnects the LEDs and makes sure that the output capacitor does not have to be charged/ discharged every PWM dimming cycle. The PWM dimming input to the $\overline{\text{FAULT}}$ pin is ANDED with the latch output of the protection circuitry to make sure that the protection circuit overrides the PWM input to the $\overline{\text{FAULT}}$ pin.

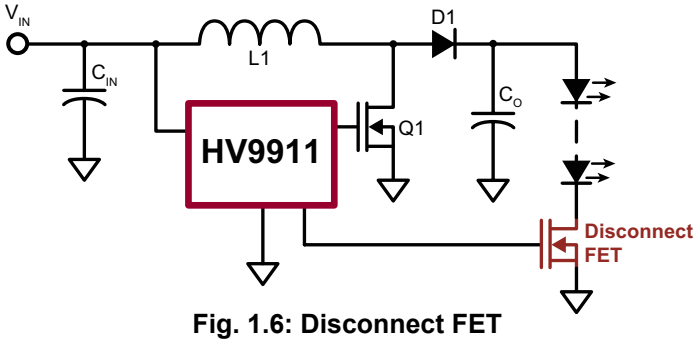


Fig. 1.6: Disconnect FET

Output short circuit protection is provided by comparing the output current sense signal (at the FDBK pin) to twice of the reference current (at the IREF pin). The output over voltage protection is activated when the voltage at the OVP pin

exceeds 1.25V. Both these signals are OR'D and this signal is fed into the latch (to give latched protection). The output of this latch turns off both the GATE pin and the $\overline{\text{FAULT}}$ pin when a fault condition occurs. Once the IC goes into the fault mode, power has to be recycled to the IC to reset the latch.

Startup with the HV9911

A couple of points have to be taken into consideration when starting up the HV9911 circuit.

- When the VDD and PWMD pins are shorted together and the circuit is turned off and on by either connecting or disconnecting the input voltage from the circuit, the capacitor at the REF pins should be limited to 0.1µF and the capacitor at the VDD pin to a value less than 1µF to ensure proper startup.

- If the circuit is going to be turned on or off with an external signal while the input voltage is always connected, then both capacitors can be increased beyond the limits mentioned above.

Linear Dimming

Linear dimming is achieved by varying the voltage level at the IREF pin. This can be done either with a potentiometer from the REF pin or from an external voltage source and a resistor divider. This allows the current to be linearly dimmed. However, note that once the voltage at the IREF pin is lowered to a very small value, the offsets of the output short circuit current comparator might cause the HV9911 fault mode to activate improperly. The power to the IC will have to be recycled to startup the circuit again. To prevent this mistrigerring, it is advisable to limit the minimum voltage at the IREF pin to about 20 – 30mV.

PWM Dimming

The features included in the HV9911 help achieve a very fast PWM dimming response in spite of the shortcomings of the boost converter. The PWM dimming signal controls three nodes in the IC.

- Gate signal to the switching FET
- Gate signal to the disconnect FET
- Output connection of the transconductance opamp

When PWMD is high, the gates of both the switching FET and the disconnect FET are enabled. At the same time, the output of the transconductance opamp is connected to the compensation network. This allows the boost converter to operate normally.

When PWMD goes low, the GATE of the switching FET is disabled to stop energy transfer from the input to the output. However, this does not prevent the output capacitor from discharging into the LEDs causing a large fall time for the LED current. This discharge of the capacitor also means that when the circuit restarts, the output capacitor has to charge again, causing an increase in the rise time of the LED current. This problem becomes more prominent with larger output capacitors. Thus, it is important to prevent the discharge of the output capacitor. This is done by turning off the disconnect FET. This causes the LED current to fall to zero almost instantaneously. Since the output capacitor does not discharge, there is no necessity to charge the capacitor when PWMD goes high. This enables a very fast rise time as well.

When PWMD goes low, the output current goes to zero. This means that the feedback amplifier sees a very large error signal across its input terminals, which would cause the voltage across the compensation capacitor to increase to the positive rail. Thus, when the PWMD signal goes high again, the large voltage across the compensation network, which dictates the peak inductor current value, will cause a large spike in the LED current. The current will come back into regulation depending on the speed of the controller. Disconnecting the output of the amplifier from the compensation network when PWMD goes low will help keep the voltage at the compensation unchanged. Thus, when PWMD goes high again, the circuit will already be at the steady state conditions eliminating the large turn-on spike in the LED current.

Designing Closed Loop Controllers

The compensation needed to stabilize the converter could be either a Type-I circuit (a simple integrator) or a Type-II circuit (an integrator with an additional pole-zero pair). The type of the compensation circuit required will be dependent on the phase of the power stage at the cross over frequency.

The loop gain of the closed loop system (Fig. 1-7) is given by:

$$\text{Loop Gain} = R_S \bullet G_M \bullet Z_C(S) \bullet \frac{1}{15} \bullet \frac{1}{R_{CS}} \qquad (1\text{-}1)$$

where G_M is the transconductance of the opamp (435µA/V), $Z_C(S)$ is the impedance of the compensation network and $G_P(S)$ is the transfer function of the power stage. Please note that although the resistors give a 1:14 ratio, the overall effect when including the diode drop is effectively 1:15.

Assume a crossover frequency for the loop gain to be f_C. Let the magnitude and phase of the power stage transfer function at this frequency be A_{PS} and $\Phi_{PS}{}^{O}$ respectively.

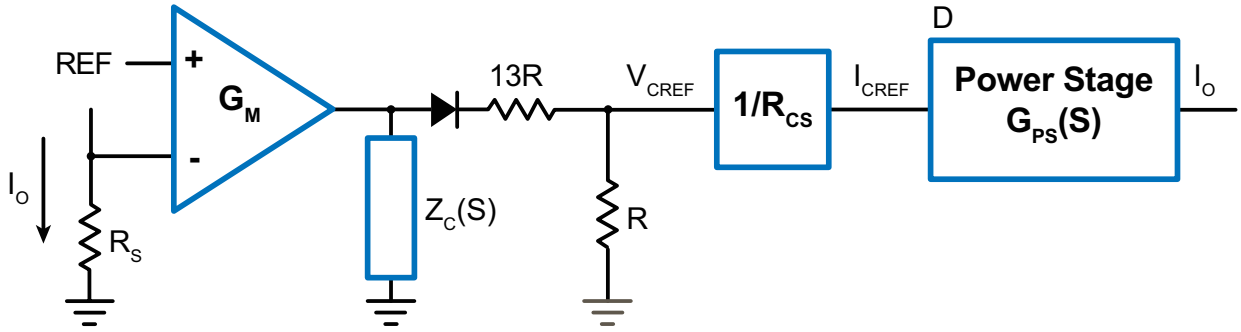


Fig. 1.7: Loop Gain of the Boost Controller

To get a phase margin of $\Phi_M{}^O$ the phase boost required will be:

$$\Phi_{BOOST} = \Phi_M - \Phi_{PS} - 90^O \quad (1\text{-}2)$$

Based on the value of the phase boost required, the type of compensation can be determined.

$$\Phi_{BOOST} \le 0^O \rightarrow \text{Type I Controller} \quad (1\text{-}3)$$

$$0^O \le \Phi_{BOOST} \le 90^O \rightarrow \text{Type II Controller}$$

$$90^O \le \Phi_{BOOST} \le 180^O \rightarrow \text{Type III Controller}$$

Type-III controllers are usually not required to compensate a HV9911 based boost LED driver, and thus will not be discussed in this application note. The implementations for the Type-I and Type-II systems for use with the HV9911 are given in Table 1.1.

Designing with Type-I controllers is simple – adjust C_C so that the magnitude of the loop gain equals 1 at the cross over frequency.

$$R_s \cdot G_m \cdot \left(\frac{1}{2 \cdot \pi \cdot f_c \cdot C_c} \cdot\right) \cdot \frac{1}{15} \cdot \frac{1}{R_{cs}} \cdot A_{ps} = 1 \quad (1\text{-}4)$$

From the above equation, the value of the capacitor C_C can be computed, assuming the other parameters are known.

The equations needed to design the Type-II controller are given below:

$$K = \tan\left(45^o + \frac{\Phi_{BOOST}}{2}\right) \quad (1\text{-}5)$$

$$\omega_z = \frac{1}{R_z \cdot C_z} = \frac{2 \cdot \pi \cdot f_c}{K} \quad (1\text{-}6)$$

$$\omega_p = \frac{C_z + C_c}{C_z \cdot C_p \cdot R_z} = (2 \cdot \pi \cdot f_c) \cdot K \quad (1\text{-}7)$$

One more equation can be obtained by equating the magnitude of the loop gain to 1 at the cross over frequency.

$$R_s \cdot G_m \cdot \left(\frac{1}{2 \cdot \pi \cdot f_c \cdot (C_z + C_c)} \cdot K\right) \cdot \frac{1}{15} \cdot \frac{1}{R_{cs}} \cdot A_{ps} = 1 \quad (1\text{-}8)$$

Equations (1-6) to (1-8) can be solved simultaneously to compute the values for R_Z, C_Z, and C_C.

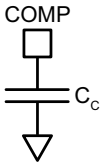
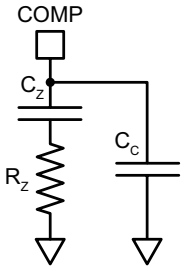
Type	Circuit Diagram	Transfer Function
I		$Z_c(s) = \frac{1}{sC_c}$
II		$Z_c(s) = \frac{1}{s(C_c + C_z)} \cdot \frac{1 + s \cdot R_z \cdot C_z}{1 + s \cdot \frac{C_z \cdot C_c}{C_z + C_c} \cdot R_z}$

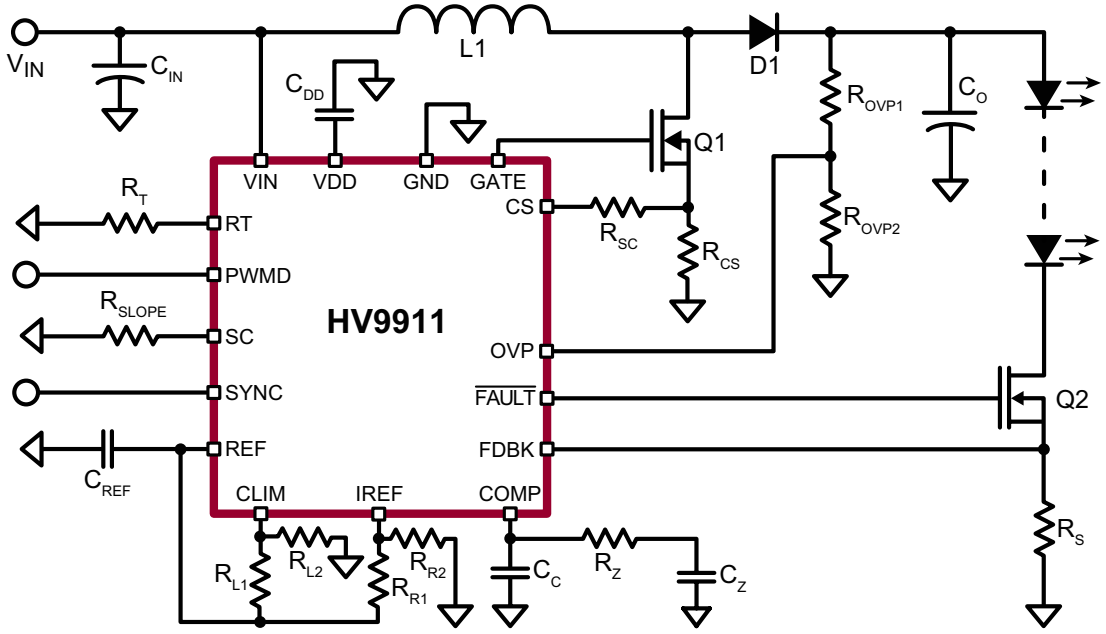
Table 1.1: Compensation Networks

Section II - Design of a Continuous Conduction Mode Boost LED Driver

Design Parameters

Parameter	Name	Value	Units
Minimum input voltage	V_{INMIN}	21	V
Maximum input voltage	V_{INMAX}	27	V
Maximum LED string voltage	V_{OMAX}	80	V
Minimum LED string voltage	V_{OMIN}	35	V
Maximum LED current	I_{OMAX}	350	mA
Minimum efficiency @	η_{MIN}	90	%
Output current ripple	ΔI_O	35	mA
Dynamic resistance of LED string	R_{LED}	22	Ω

Typical Circuit



Power Stage Design

Step 1: Select the switching frequency (f_s)

For low voltage applications (output voltage <100V), and moderate power levels (<30W), a switching frequency of f_S = 200kHz (time period T_S = 5.0µs) is a good compromise between switching power loss and size of the components. At higher voltage or power levels, the switching frequency might have to be reduced to lower the switching losses in the external FET.

Step 2: Compute the maximum duty cycle (D_{MAX})

The maximum duty cycle of operation can be computed as:

$$D_{MAX} = 1 - \frac{\eta_{MIN} \bullet V_{IN,MIN}}{V_{O,MAX}} \quad (2\text{-}1)$$

$$= 0.764$$

Note:

If D_{MAX} > 0.85, the step-up ratio is too large. The converter cannot operate in continuous conduction mode, and has to be operated in discontinuous conduction mode to achieve the required step-up ratio.

Step 3: Compute the maximum inductor current (I_{INMAX})

The maximum input current is:

$$I_{IN,MAX} = \frac{V_{O,MAX} \bullet I_{O,MAX}}{\eta_{MIN} \bullet V_{IN,MIN}} \quad (2\text{-}2)$$

$$= 1.48A$$

Step 4: Compute the input inductor (L1)

The input inductor can be computed by assuming a 25% peak-to-peak ripple in the inductor current at minimum input voltage.

$$L1 = \frac{V_{IN,MIN} \bullet D_{MAX}}{0.25 \bullet I_{IN,MAX} \bullet f} \quad (2\text{-}3)$$

$$= 216.5\mu H$$

Choose a standard 220uH inductor. To achieve 90% efficiency at the minimum input voltage, the power loss in the inductor has to around 2-3% of the total output power. Using a 3% loss in the inductor:

$$P_{IND} = 0.03 \bullet V_{O,MAX} \bullet I_{O,MAX} \quad (2\text{-}4)$$

$$= 0.84W$$

Assuming a 80% - 20% split in the inductor loss between resistive and core losses respectively, the DC resistance of the chosen inductor has to be less than:

$$DCR < \frac{0.8 \cdot P_{ind}}{(I_{in\,max})^2} \quad (2\text{-}5)$$

$$\Rightarrow DCR < 0.31\Omega$$

The saturation current of the inductor has to be at least 20% higher than its peak current.

$$I_{SAT} = 1.2 \bullet I_{IN,MAX} \bullet 1 + \frac{0.25}{2.0} \quad (2\text{-}6)$$

$$= 2.0A$$

Thus L1 is a 220µH inductor with a DC resistance about 0.3 ohms and a saturation current greater than 2.0A.

Note:

Choosing an inductor with an RMS current rating equal to $I_{IN\,MAX}$ would also yield acceptable results, although meeting the minimum efficiency requirement might not be possible.

Step 5: Choose the switching FET (Q1)

The maximum voltage across the FET in a boost converter is equal to the output voltage. Using a 20% overhead to account for switching spikes, the minimum voltage rating of the FET has to be:

$$V_{FET} = 1.2 \bullet V_{O,MAX} \quad (2\text{-}7)$$

$$= 96V$$

The rms current through the FET is:

$$I_{FET} \approx I_{IN,MAX} \bullet \sqrt{D_{MAX}} \quad (2\text{-}8)$$

$$= 1.3A$$

To get the best performance from the converter, the FET chosen has to have a current rating about 3 times the FET rms current with minimum gate charge Qg. It is recommended that for designs with the HV9911, the gate charge of the FET be less than 25nC. The FET chosen for this application is a 100V, 4.5A FET with a Qg of 11nC.

Step 6: Choose the switching Diode (D1)

The voltage rating of the diode is the same as the voltage rating of the FET (100V). The average current through the diode is equal to the maximum output current (350mA). Although the average current through the diode is only 350mA, the diode carries the full input current $I_{IN\,MAX}$ for short durations of time. The voltage drop across the diode when it is conducting will depend on the instantaneous current rather than the average current. Assuming a 1% conduction loss in the diode, the voltage drop across the diode should be less than:

$$V_f \leq \frac{0.01 \bullet V_{O,MAX} \bullet I_{O,MAX}}{I_{IN,MAX} \bullet (1\text{-}D_{MAX})} \quad (2\text{-}9)$$

$$= 0.8V$$

A schottky diode is preferable for output voltages less than 100V as these diodes do not have any reverse recovery loss associated with them. Thus, for this design, the diode chosen is a 100V, 1.0A schottky diode, which has a 0.8V forward drop at $I_{IN,MAX}$.

Step 7: Choose the output capacitor (C_o)

The value of the output capacitor depends on the dynamic resistance of the LED, the ripple current desired in the LED string and the LED current. In designs using the HV9911, a larger output capacitor (lower output current ripple) will yield better PWM dimming results.

The output stage of the boost converter is modeled in Fig. 2.1, where the LEDs are modeled as a constant voltage load with a series dynamic impedance. The output impedance (parallel combination of R_{LED} and C_O) is driven by the diode current. The waveform of the capacitor current in steady state is shown in Fig. 2.2.

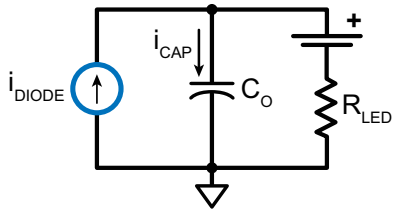


Fig. 2.1: Output Stage of the Boost Converter

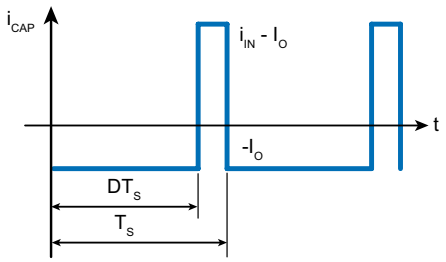


Fig. 2.2. Current through Output Capacitor

Using the 10% peak-to-peak current ripple given in the design parameters table, the maximum voltage ripple across the LED string has to be:

$$\Delta V_{P-P} = \Delta I_O \bullet R_{LED} \quad (2\text{-}10)$$
$$= 0.77V$$

Assuming a constant discharging current of 350mA when the switch is ON, the equation for the voltage ripple across the capacitor can be written as:

$$\Delta V_{P-P} = \frac{I_{OMAX} \bullet D_{MAX} \bullet T_S}{C_O} \quad (2\text{-}11)$$

Substituting values into the above equation:

$$C_O = \frac{I_{OMAX} \bullet D_{MAX}}{\Delta V_{P-P} \bullet f_S} \quad (2\text{-}12)$$
$$= 1.74\mu F$$

The rms current through the capacitor can be given by:

$$I_{RMS} = \sqrt{D_{MAX} \bullet I_{OMAX}^2 + (1 - D_{MAX})(I_{INMAX} - I_{OMAX})^2} \quad (2\text{-}13)$$
$$= 0.63A$$

In this case, a parallel combination of two 1uF, 100V metal polypropylene capacitors is chosen.

Note:
The proper type of capacitors to use are either metal film capacitors or ceramic capacitors, since they are capable of carrying this high ripple current and have low ESR. Although ceramic capacitors are smaller in size and capable of carrying the ripple current, they cause a lot of audible noise during PWM dimming. Thus metal polypropylene (or any other metal film) capacitors are the ideal choice for LED drivers if PWM dimming is required.

Step 8: Choose the disconnect FET (Q2)
The disconnect FET should have the same voltage rating as the switching FET Q1. The on-state resistance of the FET at room temperature ($R_{ON,25C}$) has to be chosen based on a 1% power loss in Q2 at full load current.

Thus:

$$R_{ON,25C} = \frac{0.01 \bullet V_{OMAX}}{I_{OMAX} \bullet 1.4} \quad (2\text{-}14)$$
$$= 1.63\Omega$$

The 1.4 factor is included to account for the increase in the on-resistance due to rise in junction temperature. In this case, a high Qg FET can be chosen if desired (as it is not switching regularly), but a high Qg FET will slow down the turn-on and turn-off times (which might be allowable based on the PWM dimming frequency). In this case, the FET chosen is a 100V, 1.5Ω, SOT-89 FET with a Qg of 5nC.

Step 9: Choose the Input capacitor (C_{IN})
The input capacitor required at the input is dictated by the stability requirements for the closed loop controller. Unfortunately, the design of the input capacitor is an iterative process.

To design this capacitor, we need to define the maximum inductance of the connection between the input source and the input of the converter $L_{SOURCE,MAX}$ (which is the sum of the two inductances shown in Fig 2.3). The maximum and minimum limits for the source resistance R_{SOURCE} (sum of the two resistors shown in Fig. 2.3) will be determined by the converter characteristics. The source inductance and resistance represent the impedance of the cables connecting the HV9911 circuit to the input power source. In order to design the input capacitors, it is necessary to have a reasonable estimation of these values. The stability of the converter will dependent on both these values.

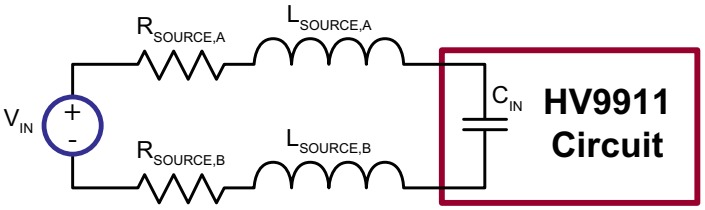


Fig. 2.3: Definition of the Source Impedance

Assume $L_{SOURCE,MAX}$ = 1.0µH (this is the maximum inductance of a 1 foot long, 22AWG cable connected to both the source and return terminals of the HV9911 circuit). The next step is to choose an LC resonant frequency f_{LC}. As a starting point, choose:

$$f_{LC} = 0.4 \bullet f_S = 80kHz \quad (2\text{-}15)$$

Then the minimum input capacitor value can be computed as:

$$C_{in} = \frac{1}{(2 \cdot \pi \cdot f_{LC})^2 \cdot L_{source,max}} \quad (2\text{-}16)$$
$$= 3.95\mu F$$

In this case, the capacitor chosen is a parallel combination of two 2.2µF, 50V ceramic capacitors.

The magnitude of the reflected converter filter impedance at the LC resonant frequency is given by:

$$R_{eq} = (1 - D_{max})^2 \cdot R_{LED} \quad (2\text{-}17)$$

$$Z_{DC} = \frac{R_{eq}}{1} \cdot \frac{\sqrt{\left[1 - (2 \cdot \pi \cdot f_{Lc})^2 \cdot \frac{L_1 \cdot C_o}{(1 - D_{max})^2}\right]^2 + \left[(2 \cdot \pi \cdot f_{Lc}) \cdot \frac{L_1}{R_{eq}}\right]^2}}{\sqrt{1 + \left[(2 \cdot \pi \cdot f_{Lc}) \cdot R_{LED} \cdot C_o\right]^2}}$$

In this case, Z_{DC} = 110Ω. For the converter to be stable, the magnitude of the impedance of the L-C combination should be less than Z_{DC}. This gives rise to the following condition on the minimum source resistance.

$$R_{source,min} = \left(\frac{L_{source,max}}{C_{in}}\right) \cdot \frac{1}{Z_{DC}} \quad (2\text{-}19)$$
$$= 2m\Omega$$

The maximum source resistance is given by:

$$R_{SOURCE,MAX} = (1 - D_{MAX})^2 \bullet R_{LED} \quad (2\text{-}20)$$
$$= 1.25\Omega$$

As can be seen from the above equations, the maximum source resistance is independent of the input filter parameters and thus there is no control over it. However, the minimum source resistance is a function of the input filter parameters.

The computed minimum value of source resistance is 2.0mΩ. This is a very small value which can easily be met. However, in some cases, the minimum source resistance might be larger than the expected resistance of the cabling. In such cases, either a small resistance can be introduced in the input line (to provide the necessary damping) or the LC resonant frequency has to be reduced and the computations carried out till the minimum source resistance is less than the expected resistance.

Note:
The source inductance can be reduced significantly by twisting the input cables together.

HV9911 Controller Design

Step 10: Choosing the timing resistor (R_T)

The timing resistor can be chosen by using:

$$\frac{1}{f_S} \approx R_T \bullet 11pF \quad (2\text{-}21)$$

In this case, for a constant 200kHz switching frequency, the timing resistor value works out to 453kΩ. This resistor needs to be connected between the RT pin and GND as shown in the typical circuit.

Step 11: Choose the two current sense resistors (R_{cs} and R_S)

The output current sense resistor is chosen by limiting the power dissipation in it to about 0.15W, so that a 1/4W resistor can be used. Using this criterion:

$$R_S = \frac{0.15W}{I_{OMAX}^2} \quad (2\text{-}22)$$
$$= 1.22\Omega$$

In this case, the resistor chosen is a 1.24Ω, 1/4W, 1% resistor.

The FET current sense resistor R_{CS} is chosen by limiting the voltage across the resistor to about 250mV at maximum input current.

$$R_{CS} = \frac{0.25}{1.125 \bullet I_{INMAX}} \quad (2\text{-}23)$$
$$= 0.15\Omega$$

The power dissipated in this resistor is:

$$P_{RCS} = I_{FET}^2 \bullet R_{CS} \quad (2\text{-}24)$$
$$= 0.25W$$

Thus, the chosen current sense resistor is a 0.15Ω, 1/2W, 1% resistor.

Step 12: Selecting the current reference resistors (R_{r1} and R_{r2})

The voltage at the current reference pin IREF can be set either by using the reference voltage provided at the REF pin (through a voltage divider) or with an external voltage source. In the present design, it is assumed that the voltage at the IREF pin is set using a voltage divider from the REF pin. The current reference resistors R_{ref1} and R_{ref2} can be computed using the following two equations:

$$R_{R1} + R_{R2} = \frac{1.25V}{50\mu A} = 25k\Omega \quad (2\text{-}25)$$

$$\frac{1.25V}{R_{R1} + R_{R2}} \bullet R_{R2} = I_{OMAX} \bullet R_S \quad (2\text{-}26)$$

For this design, the values of the two resistors selected are:

R_{R2} = 8.66kΩ, 1/8W, 1%
R_{R1} = 16.2kΩ, 1/8W, 1%

Step 13: Programming the slope compensation (R_{SLOPE} and R_{SC})

Since the boost inductor being designed is operating at constant frequency, slope compensation is required to ensure the stability of the converter. The slope added to the current sense signal has to be one-half the maximum down slope of the inductor current to ensure stability of the peak current mode control scheme for all operating conditions. This can easily be achieved by the proper selection of the two slope compensation resistors R_{SLOPE} and R_{SC}.

For the present design, the maximum down slope of the inductor current is:

$$DS = \frac{V_{OMAX} - V_{INMIN}}{L1} \quad (2\text{-}27)$$

$$= 0.268A/\mu s$$

The programming resistors can then be chosen as:

$$R_{SC} = \frac{R_{slope} \cdot DS(A/\mu s) \cdot 10^6 \cdot R_{cs}}{10 \cdot f_s} \quad (2\text{-}28)$$

Assuming R_{SLOPE} = 49.9kΩ,

$$R_{SC} = \frac{49.9k \cdot 0.2682 \cdot 10^6 \cdot 0.15}{10 \cdot 200k} \quad (2\text{-}29)$$

$$= 1k\Omega$$

The selected resistor values are:

R_{SC} = 1.0kΩ, 1/8W, 1%
R_{SLOPE} = 49.9kΩ, 1/8W, 1%

Note:
The maximum current that can be sourced out of the SC pin is limited to 100µA. This limits the minimum value of the R_{SLOPE} resistor to 25kΩ. It is recommended that R_{SLOPE} be chosen in the range of 25kΩ - 50kΩ.

Step 14: Setting the inductor current limit ($R_{L1}$and R_{L2})

The inductor current limit value depends on two factors - the maximum inductor current and the slope compensation signal added to the sensed current. The current limit is set by another resistor divider from the REF pin. The voltage at the CLIM pin can be computed as:

$$V_{CLIM} \geq 1.35 \bullet I_{INMAX} \bullet R_{CS} + \frac{4.5 \bullet R_{SC}}{R_{SLOPE}} \quad (2\text{-}30)$$

This equation assumes that the current limit level is set at about 120% of the maximum inductor current $I_{IN\,MAX}$ and that the operating duty cycle is at 90% (the maximum for the HV9911).

For this design:

$$V_{CLIM} = 1.35 \bullet 1.48 \bullet 0.15 + \frac{4.5 \bullet 1000}{49.0k\Omega} \quad (2\text{-}31)$$

$$= 0.39V$$

Using a maximum current sourced out of REF pin of 50µA (similar to Step 12), the two resistors can be chosen as:

R_{L1} = 17.4kΩ, 1/8W, 1%
R_{L2} = 7.87kΩ, 1/8W, 1%

Note:
It is recommended that no capacitor be connected at the CLIM pin.

Step 15: Capacitors at V_{DD} and REF pins ($C_{REF}$and C_{DD})

It is recommended that bypass capacitors be connected to both pins. For the VDD pin, the capacitor used is a 1.0µF ceramic chip capacitor. If the design uses high gate charge switching FETs (Qg > 15nC), the capacitor at the VDD pin should be increased to 2.2µF.

For the REF pin, the capacitor used is a 0.1µF ceramic chip capacitor.

Step 16: Setting the Over-voltage Trip Point (R_{OVP1} and R_{OVP2})

The over-voltage trip point can be set at a voltage 15% higher than the maximum steady state voltage. Using a 15% margin, the maximum output voltage during open LED condition will be

$$V_{OPEN} = 1.15 \bullet V_{OMAX} \quad (2\text{-}32)$$

$$= 92V$$

Then, the resistors that set the over-voltage set point can be computed as:

$$R_{OVP1} = \frac{(V_{OPEN} - 1.25)^2}{0.1} \quad (2\text{-}33)$$

$$= 82.36k\Omega$$

The above equation will allow us to select a 1/8W resistor by limiting the power dissipation in the resistor.

$$R_{OVP2} = \frac{R_{OVP1}}{(V_{open} - 1.25)} \cdot 1.25V \quad (2\text{-}34)$$

$$= 1.13k\Omega$$

The closest 1% resistor values are:

R_{OVP1} = 82.5kΩ, 1/8W, 1%
R_{OVP2} = 1.13kΩ, 1/8W, 1%

Note:
The actual over-voltage point will vary from the desired point by ±3% due to the variation in the reference (see datasheet). For this design, it varies from 89.25V to 94.75V.

Step 17: Designing the Compensation Network

For the continuous conduction mode boost converter in peak current control mode and for frequencies less than 1/10th of the switching frequency, the power stage transfer function is given by:

$$G_{ps}(s) = \frac{(1-D_{max})}{2} \cdot \frac{1 - s \cdot \frac{L1}{(1-D_{max})^2 \cdot R_{LED}}}{1 + s \cdot \frac{R_{LED} \cdot C_o}{2}} \quad (2\text{-}35)$$

For the present design, choose a crossover frequency f_C = 2.0kHz. The low crossover frequency will result in large values for C_C and C_Z, which will indirectly provide a soft-start for the circuit. Since the HV9911 does not depend on the speed of the controller circuit for the PWM dimming response, the low crossover frequency will not have an adverse effect on the PWM dimming rise and fall times.

At this frequency, the magnitude and frequency of the power stage transfer function (obtained by substitutings = i•(2π•f_C) in (2-35)) are:

$$\left|G_{ps}(s)\right|_{fc=2kHz} = A_{ps} = 0.283$$
$$\angle G_{ps}(s)\Big|_{fc=2kHz} = \phi_{ps} = -80^\circ \quad (2\text{-}36)$$

To get a phase margin of about Φ_M = 45° (the recommended phase margin range is 45°- 60°), the phase boost required will be:

$$\Phi_{BOOST} = \Phi_M - \Phi_{PS} - 90^O = 35^O \quad (2\text{-}37)$$

From (1-3), we can see that a Type-II system is required to stabilize the system. Using (1-5) to (1-8), the values of the compensation network can be computed.

The equations needed to design the Type-II controller are given below:

$$K = \tan\left(45^O + \frac{\Phi_{BOOST}}{2}\right) \quad (2\text{-}38)$$

$$\omega_z = \frac{1}{R_z \cdot C_z} = \frac{2 \cdot \pi \cdot f_c}{K} = 6605 \ \ rad/sec \quad (2\text{-}39)$$

$$\omega_p = \frac{C_z + C_p}{C_z \cdot C_p \cdot R_z} = (2 \cdot \pi \cdot f_c) \cdot K = 23910 \ \ rad/sec \quad (2\text{-}40)$$

One more equation can be obtained by equating the magnitude of the loop gain to 1 at the cross over frequency.

$$R_s \cdot G_m \cdot \left(\frac{1}{2 \cdot \pi \cdot f_c \cdot (C_z + C_c)} \cdot K\right) \cdot \frac{1}{15} \cdot \frac{1}{R_{cs}} \cdot A_{ps} = 1 \quad (2\text{-}41)$$

From (2-41),

$C_Z + C_C$ = 10nF

$$C_C = 10nF - C_Z \quad (2\text{-}42)$$

Substituting (2-39) and (2-42) into (2-40),

$$C_c = (C_z + C_c) \cdot \frac{\omega_z}{\omega_p} = 2.84nF \quad (2\text{-}43)$$

From (2-43) and (2-41),

$$C_Z = 7.43nF \quad (2\text{-}44)$$

From (2-39) and (2-44),

$$R_Z = \frac{1}{\omega_Z \bullet C_Z} = 20.37k\Omega \quad (2\text{-}45)$$

Choose:

C_C = 2.2nF, 50V, C0G capacitor
C_Z = 6.8nF, 50V, C0G capacitor
R_Z = 20.0kΩ, 1/8W, 1% resistor

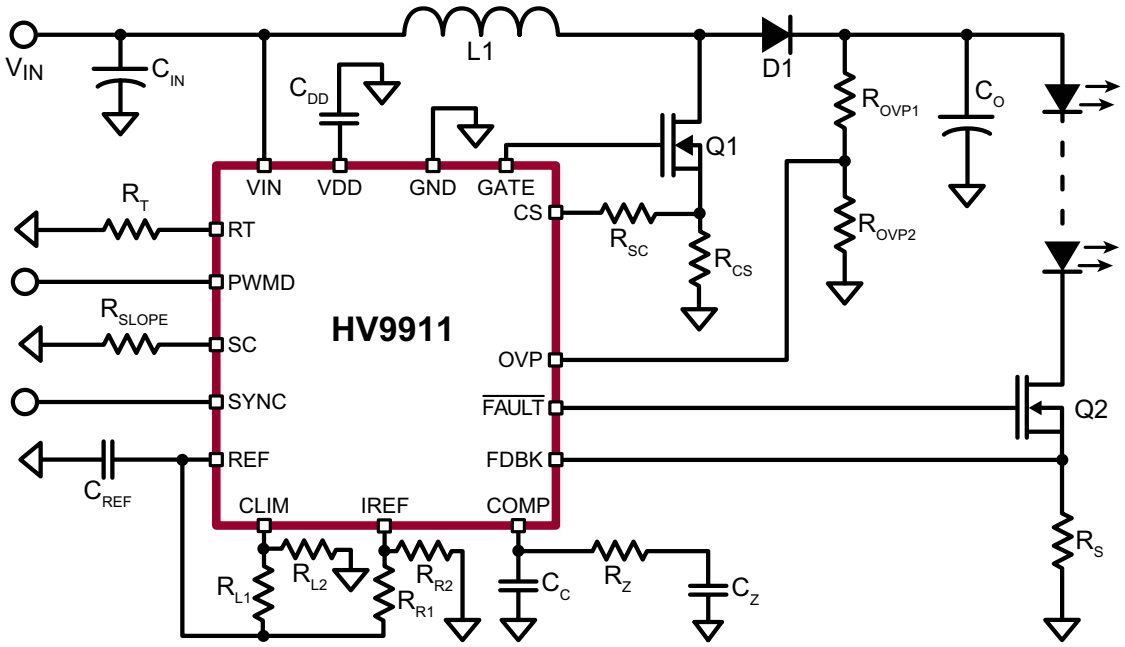
This completes the design of the HV9911 based Boost Converter operating in Continuous Conduction Mode.

Section III - Design of a Discontinuous Conduction Mode Boost LED Driver

Design Parameters

Parameter	Name	Value	Units
Minimum input voltage	V_{INMIN}	9	V
Maximum input voltage	V_{INMAX}	16	V
Maximum LED string voltage	V_{OMAX}	80	V
Minimum LED string voltage	V_{OMIN}	35	V
Maximum LED current	I_{OMAX}	120	mA
Minimum efficiency @	η_{MIN}	85	%
Output current ripple	ΔI_O	12	mA
Dynamic resistance of LED string	R_{LED}	60	Ω

Typical Circuit



Power Stage Design

Step 1: Select the switching frequency (f_s)

For low voltage applications (output voltage <100V), and moderate power levels (<30W), a switching frequency of f_S = 200kHz is a good compromise between switching power loss and size of the components. At higher voltage or power levels, the switching frequency might have to be reduced to lower the switching losses in the external FET.

Step 2: Compute the maximum inductor current ($I_{IN\ MAX}$)

The maximum input current is:

$$I_{IN,MAX} = \frac{V_{O,MAX} \cdot I_{O,MAX}}{\eta_{MIN} \cdot V_{IN,MIN}} \qquad (3\text{-}1)$$

$$= 1.255A$$

Step 3: Compute the input inductor (L1)

The variation in the switching frequency for the HV9911 is typically ±12%. Thus, the maximum switching frequency is $f_{S,MAX}$. The inductor value has to be computed using this frequency, since the converter has to be designed so that it does not go into CCM under any conditions.

Assuming that the sum of the on-time of the switch and the on-time of the diode is 95% of the total switching time period at $V_{IN,MIN}$ and $f_{S,MAX}$:

$$L1 \cdot i_{Lpk(fsmax)} \cdot \left(\frac{1}{V_{inmin}} + \frac{1}{V_{omax} - V_{inmin}} \right) = \frac{0.95}{f_{s,max}} \qquad (3\text{-}2)$$

$$= 4.24\mu s$$

where i_{Lpk} is the peak input current (Fig. 3-1).

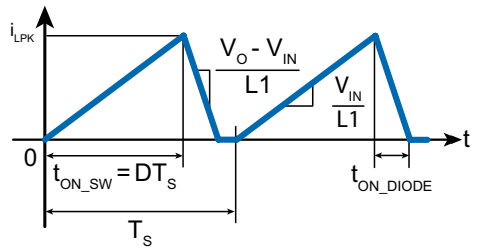


Fig. 3.1: Inductor Current Waveform in DCM

The average input current at the minimum input voltage is equal to the average inductor current and can be computed from:

$$I_{IN,MAX} = \frac{1}{2} \cdot I_{LPK(fs,MAX)} \cdot 0.95 \quad (3\text{-}3)$$

$$= 0.475 \cdot I_{LPK(fs,MAX)}$$

Using (3-1) and (3-3), the peak input current is:

$$I_{LPK(fs,MAX)} = \frac{I_{IN,MAX}}{0.475} \quad (3\text{-}4)$$

$$\approx 2.64A$$

Substituting for i_{Lpk} in (3-2):

$$L1 = \frac{0.95}{224k} \cdot \frac{9V \cdot (80V - 9V)}{80V \cdot 2.64A} \quad (3\text{-}5)$$

$$= 12.82\mu H$$

Note that the value of L1 computed is the absolute maximum value for the inductor. Assuming a ±20% variation in the inductance, the nominal inductor value has to be:

$$L1_{NOM} = \frac{L1}{1.2} \quad (3\text{-}6)$$

$$= 10.69\mu H$$

The closest standard value is a 10µH inductor. The current ratings for the inductor are computed at the nominal switching frequency.

$$i_{Lpk} = \sqrt{\frac{2 \cdot I_{in\max}}{f_s \cdot L1_{nom} \cdot \left(\frac{1}{V_{in\min}} + \frac{1}{V_{o\max} - V_{in\min}} \right)}} \quad (3\text{-}7)$$

$$= 3.2A$$

The on-time of the switch can be computed as:

$$t_{ON\_SW} = \frac{L1_{NOM} \cdot I_{LPK}}{V_{IN,MIN}} \quad (3\text{-}8)$$

$$= 3.52\mu s$$

The on-time of diode is:

$$t_{ON\_DIODE} = \frac{L1_{NOM} \cdot I_{LPK}}{V_{O,MAX} - V_{IN,MIN}} \quad (3\text{-}9)$$

$$= 446ns$$

The maximum duty cycle can then be computed as:

$$D_{MAX} = t_{ON\_SW} \cdot f_S \quad (3\text{-}10)$$

$$= 0.71$$

The diode conduction time ratio can be expressed as:

$$D1 = t_{ON\_DIODE} \cdot f_S \quad (3\text{-}11)$$

$$= 0.09$$

The rms current through the inductor is:

$$I_{Lrms} = i_{Lpk} \cdot \sqrt{\frac{D_{max} + D1}{3}} \quad (3\text{-}12)$$

$$= 1.63A$$

Choose a 10µH inductor (+/-20% tolerance). A custom inductor would work best for this application given the large swings in the inductor flux. However, if a standard value inductor is preferred, the saturation current rating of the inductor should be at least 1.5 times the peak current, computed in (3-4) to keep the core losses to an acceptable value.

The inductor chosen in this case is a 10µH inductor with an rms current rating of 1.6A and a saturation current rating of 4.8A.

Step 4: Choose the switching FET (Q1)

The maximum voltage across the FET in a boost converter is equal to the output voltage. Using a 20% overhead to account to switching spikes, the minimum voltage rating of the FET has to be:

$$V_{FET} = 1.2 \cdot V_{O\,MAX} \quad (3\text{-}13)$$

$$= 96V$$

The rms current through the FET is:

$$I_{FET} \approx i_{Lpk} \cdot \sqrt{\frac{D_{max}}{3}} \quad (3\text{-}14)$$

$$= 1.53A$$

To get the best performance from the converter, the FET chosen has to have a current rating about 3 times the FET rms current with minimum gate charge Qg. It is recommended that for designs with the HV9911, the gate charge of the FET be less than 25nC.

The FET chosen for this application is a 100V, 4.5A FET with a Qg of 11nC.

Step 6: Choose the switching Diode (D1)

The voltage rating of the diode is the same as the voltage rating of the FET (100V). The average current through the diode is equal to the maximum output current (350mA). Although the average current through the diode is only 350mA, the peak current through the diode is equal to I_{Lpk}. The voltage drop across the diode when it is conducting will depend on the instantaneous current rather than the average current. Assuming a 2% conduction loss in the diode, the voltage drop across the diode should be less than:

$$V_f \le \frac{2 \cdot 0.02 \cdot V_{omax} \cdot I_{omax} \cdot T_s}{t_{on\_diode} \cdot i_{Lpk}} \quad (3\text{-}15)$$

$$= 1.3V$$

A schottky diode is preferable for output voltages less than 100V as these diodes do not have any reverse recovery loss associated with them. Thus, for this design, the diode chosen is a 100V, 1.0A schottky diode, which has a 1.2V forward drop at I_{Lpk}.

Step 7: Choose the output capacitor (C_O)

The value of the output capacitor depends on the dynamic resistance of the LED string as well as the ripple current desired in the LED string. In designs using the HV9911, a larger output capacitor (lower output current ripple) will yield better PWM dimming results.

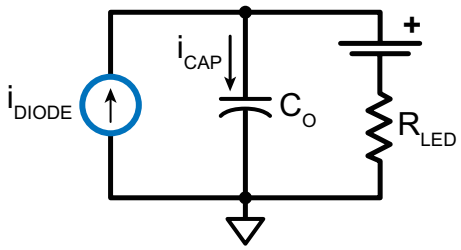


Fig. 3.2: Output Stage of the Boost Converter

The output stage of the boost converter is modeled in Fig. 3.2, where the LEDs are modeled as a constant voltage load with a series dynamic impedance. The waveform of the capacitor current in steady state is shown in Fig. 3-3.

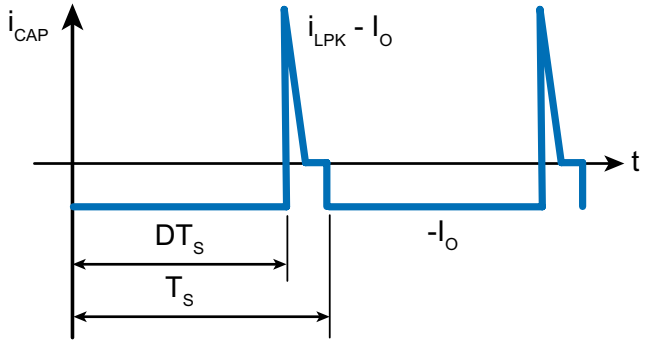


Fig. 3.3: Capacitor Current Waveform

Using the 10% peak-to-peak current ripple given in the design parameters table, the maximum voltage ripple across the LED string has to be

$$\Delta V_{P\text{-}P} = \Delta I_O \bullet R_{LED} \quad (3\text{-}16)$$
$$= 0.72V$$

Assuming a constant discharging current of 350mA when the diode current is zero, the equation for the voltage ripple across the capacitor can be written as:

$$I_{O\,MAX} = \frac{C_O \bullet \Delta V_{P\text{-}P}}{D_{MAX} \bullet T_S} \quad (3\text{-}17)$$

Substituting values into the above equation:

$$C_O = \frac{I_{O\,MAX} \bullet D_{MAX}}{\Delta V_{P\text{-}P} \bullet T_S} \quad (3\text{-}18)$$

$$= 0.58\mu F$$

The rms current through the capacitor can be given by:

$$I_{rms} = \sqrt{(1-D1) \cdot I_{omax}{}^2 + \frac{D1}{3} \cdot (i_{Lpk} - I_{omax})^2} \quad (3\text{-}19)$$
$$= 0.54A$$

In this case, a 2.2µF, 100V metal polypropylene capacitor is chosen.

Note:

The proper type of capacitors to use are either metal film capacitors or ceramic capacitors, since they are capable of carrying this high ripple current and have low ESR. Although ceramic capacitors are smaller in size and capable of carrying the ripple current, they cause a lot of audible noise during PWM dimming. Thus metal polypropylene (or any other metal film) capacitors are the ideal choice for LED drivers if PWM dimming is required.

Step 8: Choose the disconnect FET (Q2)

The disconnect FET should have the same voltage rating as the switching FET Q1. The on-state resistance of the FET at room temperature ($R_{ON,25C}$) has to be chosen based on a 1% power loss in Q2 at full load current. Thus:

$$R_{ON,25C} = \frac{0.01 \bullet V_{O\,MAX}}{I_{O\,MAX} \bullet 1.4} \quad (3\text{-}20)$$

The 1.4 factor is included to account for the increase in the on-resistance due to rise in junction temperature. In this case, a high Qg FET can be chosen if desired (as it is not switching regularly), but a high Qg FET will slow down the turn-on and turn-off times (which might be allowable based on PWM dimming frequency). In this case, the FET chosen is a 100V, 0.7Ω, SOT-23 FET with a Qg of 2.9nC.

Step 9: Choose the Input capacitor (C_{IN})

The input capacitor required at the input is dictated by the stability requirements for the closed loop controller. Unfortunately, the design of the input capacitor is an iterative process.

To design this capacitor, we need to define the maximum inductance of the connection between the input source and the input of the converter $L_{SOURCE,MAX}$ (which is the sum of the two inductances shown in Fig. 3.4). The maximum and minimum limits for the source resistance R_{SOURCE} (sum of the two resistors shown in Fig. 3.4) will be determined by the converter characteristics. The source inductance and resistance represent the impedance of the cables connecting the HV9911 circuit to the input power source. In order to design the input capacitors, it is necessary to have a reasonable estimation of these values. The stability of the converter will dependent on both these values.

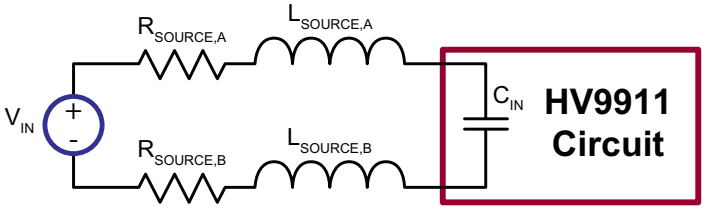


Fig. 3.4: Definition of the Source Impedance

Assume $L_{SUORCE,MAX}$ = 1.0µH (this is the maximum inductance of a 1 foot long, 22AWG cable connected to both the source and return terminals of the HV9911 circuit). The next step is to choose an LC resonant frequency f_{LC}. As a starting point, choose:

$$f_{LC} = 0.4 \bullet f_S \qquad (3\text{-}21)$$

Then the minimum input capacitor value can be computed as:

$$C_{IN} = \frac{1}{(2\pi \bullet f_{LC})2 \bullet L_{SOURCE,MAX}} \qquad (3\text{-}22)$$

$$= 3.95\mu F$$

In this case, the capacitor chosen is a parallel combination of two 2.2µF, 25V ceramic capacitors.

The magnitude of the reflected converter filter impedance at the LC resonant frequency is given by substituting s = i • 2π • f_{LC} into (3-23) and taking the magnitude of the resultant complex number.

$$M = \frac{V_{o\max}}{V_{in\min}}$$

$$Z_{DC}(s) = s \cdot L_1 - \frac{R_{LED} / M^2}{\frac{M-2}{M-1} + \frac{1}{(2 \cdot M - 1) + s \cdot R_{LED} \cdot C_o \cdot (M-1)}} \qquad (3\text{-}23)$$

In this case, $|Z_{DC}|$ = 5.1Ω. For the converter to be stable, the impedance of the L-C combination should be less than Z_{DC}. This gives rise to one condition on the minimum source resistance.

$$R_{source,min} = \left(\frac{L_{source,max}}{C_{in}}\right) \cdot \frac{1}{Z_{DC}} \qquad (3\text{-}24)$$

$$= 44m\Omega$$

The maximum source resistance is given by:

$$R_{source,max} = \frac{M-1}{M^2 \cdot (M-2)} \cdot R_{LED} \qquad (3\text{-}25)$$

$$= 0.846\Omega$$

As can be seen from the above equations, the maximum source resistance is independent of the input filter parameters and thus there is no control over it. However, the minimum source resistance is a function of the input filter parameters.

The computed minimum value of source resistance is 44mΩ. This is a small value which can easily be met. However, in some cases, the minimum source resistance might be larger than the expected resistance of the cabling. In such cases, either a small resistance can be introduced in the input line (to provide the necessary damping) or the LC resonant frequency has to be reduced and the computations carried out till the minimum source resistance is less than the expected resistance.

Note:

The source inductance can be reduced significantly by twisting the input cables together.

HV9911 Controller Design

Step 10: Choosing the timing resistor (R_T)

The timing resistor can be chosen by using:

$$\frac{1}{f_S} \approx RT \bullet 11pF \qquad (3\text{-}26)$$

In this case, for a constant 200kHz switching frequency, the timing resistor value works out to 453kΩ. This resistor needs to be connected between the RT pin and GND as shown in the typical circuit.

Step 11: Choose the two current sense resistors (R_{CS} and R_S)

The output current sense resistor is chosen by limiting the power dissipation in it to about 0.06W, so that a 1/8W resistor can be used. Using this criterion,

$$R_S = \frac{0.06W}{I_{O\,MAX}^2} \quad (3\text{-}27)$$

$$= 4.17\Omega$$

In this case, the resistor chosen is a 3.33Ω, 1/8W, 1%.

The FET current sense resistor R_{CS} is chosen by limiting the voltage across the resistor to about 250mV at maximum input current.

$$R_{CS} = \frac{0.25}{I_{LPK}} \quad (3\text{-}28)$$

$$= 0.08\Omega$$

The power dissipated in this resistor is:

$$P_{RCS} = I_{FET}^2 \bullet R_{CS} \quad (3\text{-}29)$$

$$= 0.19W$$

Thus, the chosen current sense resistor is 0.08Ω, 1/4W, 1%.

Step 12: Selecting the current reference resistors (R_{R1} and R_{R2})

The voltage at the current reference pin IREF can be set either by using the reference voltage provided at the REF pin (through a voltage divider) or with an external voltage source. In the present design, it is assumed that the voltage at the IREF pin is set using a voltage divider from the REF pin. The current reference resistors R_{REF1} and R_{REF2} can be computed using the following two equations:

$$R_{R1} + R_{R2} = \frac{1.25V}{50\mu A} = 25k\Omega \quad (3\text{-}30)$$

$$\frac{1.25V}{R_{R1} + R_{R2}} \bullet R_{R2} = I_{O\,MAX} \bullet R_S \quad (3\text{-}31)$$

For this design, the values of the two resistors can be computed to be:

R_{R2} = 7.87kΩ, 1/8W, 1%
R_{R1} = 16.9kΩ, 1/8W, 1%

Step 13: Setting the inductor current limit (R_{L1} and R_{L2})

The inductor current limit value depends on two factors – the maximum inductor current and the slope compensation signal added to the sensed current. The current limit is set by another resistor divider from the REF pin. The voltage at the CLIM pin can be computed as:

$$V_{CLIM} \geq 1.2 \bullet I_{LPK} \bullet R_{CS} \quad (3\text{-}32)$$

This equation assumes that the current limit level is set at about 120% of the maximum inductor current $I_{IN\,MAX}$.

For this design:

$$V_{CLIM} = 1.2 \bullet 3.2 \bullet 0.08 \quad (3\text{-}33)$$

$$= 0.3V$$

Using a maximum current sourced out of REF pin of 50µA (similar to Step 12), the two resistors can be chosen as:

R_{L1} = 19.1kΩ, 1/8W, 1%
R_{L2} = 6.04kΩ, 1/8W, 1%

Note:
It is recommended that no capacitor be connected at the CLIM pin.

Step 14: Capacitors at VDD and REF pins (C_{REF} and C_{DD})

It is recommended that bypass capacitors be connected to both pins. For the V_{DD} pin, the capacitor used is a 1µF ceramic chip capacitor. If the design uses high gate charge switching FETs (Qg > 15nC), the capacitor at the V_{DD} pin should be increased to 2.2µF.

For the REF pin, the capacitor used is a 0.1µF ceramic chip capacitor.

Step 15: Setting the Over-voltage Trip Point (R_{OVP1} and R_{OVP2})

The over-voltage trip point can be set at a voltage 15% higher than the maximum steady state voltage. Using a 15% margin, the maximum output voltage during open LED condition will be:

$$V_{OPEN} = 1.15 \bullet V_{O\,MAX} \quad (3\text{-}34)$$

$$= 92V$$

Then, the resistors which set the over-voltage set point can be computed as:

$$R_{OVP1} = \frac{(V_{OPEN} - 1.25)^2}{0.1} \quad (3\text{-}35)$$

$$= 82.36k\Omega$$

The above equation will allow us to select a 1/8W resistor by limiting the power dissipation in the resistor.

$$R_{OVP2} = \frac{R_{OVP1}}{(V_{OPEN} - 1.25)} \bullet 1.25V \quad (3\text{-}36)$$

The closest 1% resistor values are:

R_{OVP1} = 82.5kΩ, 1/8W, 1%
R_{OVP2} = 1.13kΩ, 1/8W, 1%

Note:
The actual over-voltage point will vary from the desired point by ±3% due to the variation in the reference (see datasheet). For this design, it varies from 89.25 to 94.75V.

Step 16: Designing the Compensation Network

To compute the transfer function for the discontinuous conduction mode boost converter in peak current control mode, we need to define a couple of factors.

$$M = \frac{V_{O\,MAX}}{V_{IN\,MIN}} \quad (3\text{-}37)$$

$$G_R = \frac{M - 1}{2M - 1} \quad (3\text{-}38)$$

For frequencies less than 1/10th of the switching frequency, the power stage transfer function is given by:

$$G_{ps}(s) = 2 \cdot \frac{I_{omax}}{i_{Lpk}} \cdot \frac{G_R}{1 + s \cdot R_{LED} \cdot C_o \cdot G_R} \quad (3\text{-}39)$$

For the present design, choose a crossover frequency f_C = 2.0kHz. The low crossover frequency will result in large values for C_Z and C_C, which will indirectly provide a soft-start for the circuit. Since the HV9911 does not depend on the speed of the controller circuit for the PWM dimming response, the low crossover frequency will not have an adverse effect on the PWM dimming rise and fall times.

At this frequency, the magnitude and frequency of the power stage transfer function (obtained by substituting $s = I(2\pi \bullet f_{LC})$ in (3-39)) are:

$$\left|G_{ps}(s)\right|_{fc=10kHz} = A_{ps} = 0.035$$
$$\angle G_{ps}(s)\Big|_{fc=10kHz} = \phi_{ps} = -11.7^\circ \quad (3\text{-}40)$$

To get a phase margin of about Φ_M = 45° (the recommended phase margin range is 45°- 60°), the phase boost required will be:

$$\phi_{boost} = \phi_m - \phi_{ps} - 90^\circ = -32^\circ \quad (3\text{-}41)$$

For the present design, a simple Type-I controller will suffice (from (1-3)). All that is needed is to adjust the gain of the loop gain to be 1 at the cross over frequency.

Using Equation (1-4) to design the capacitor C_C:

$$R_s \cdot G_m \cdot \left(\frac{1}{2 \cdot \pi \cdot f_c \cdot C_c} \cdot\right) \cdot \frac{1}{15} \cdot \frac{1}{R_{cs}} \cdot A_{ps} = 1 \quad (3\text{-}42)$$

From the above equation:

C_C = 2.68nF (3-43)

Choose:

C_C = 2.7nF, 50V, C0G capacitor

This completes the design of the HV9911 based Boost Converter operating in Discontinuous Conduction Mode.

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