Driving a High Voltage Pulser with the MD1811

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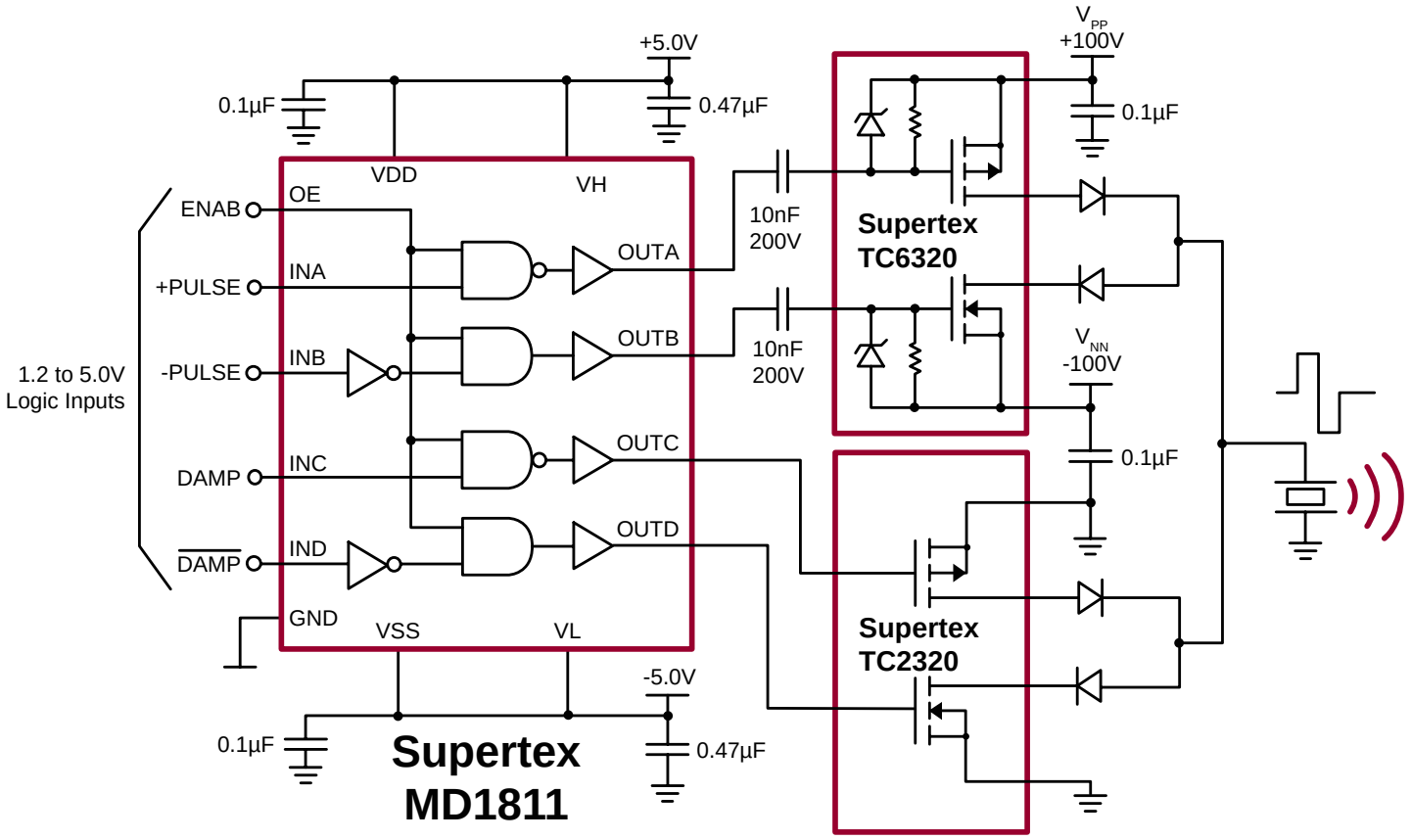
Introduction

Applications as diverse as medical ultrasound imaging, flaw detection for material screening, and Sonar transponders demand high-speed, high-voltage pulse generation at relatively high output currents. This application note describes how the Supertex MD1811 quad-channel ultrasound driver and two proprietary DMOS transistor pairs achieve excellent performance in a pulser application using minimum components.

The circuit in **Figure 1** produces bipolar return-to-zero pulses of -100 to +100V with rise and fall times of less than 15ns while sinking and sourcing 2.0A or more. Eliminating the need for a separate logic supply, the MD1811 can operate from a single 5.0 to 12V rail, with CMOS-compatible logic inputs controlling its outputs from a 1.2 to 5.0V logic interface.

A unipolar 0 to +200V pulser appears in **Figure 2**, while **Figure 3** shows a 0 to -200V version.

Figure 1. MD1811 Driving a ±100V Bipolar Pulser



Circuit Description

High voltage pulser circuits always comprise four basic stages: an input signal interface, a voltage level translator, a high-current gate-drive buffer, and the high-voltage, high-current output MOSFETs. The MD1811 integrates four channels of the first three stages into a 16-Lead QFN package.

Low input capacitance and fast switching speed are the important features of the MD1811's input stage. Its logic inputs have an input impedance of about 20kΩ in parallel with 5.0pF, and an internal speed of around 100MHz.

The output enable pin OE serves two purposes:

1) Its logic-high state determines the threshold voltage for the input-channel level translators. The MD1811's input stage logic is fully compatible with 1.8, 2.0, 2.5, 3.3, or 5.0V CMOS logic. The level translators are also compatible with these logic voltage levels right up to the MOSFETs' gate-driver voltage level, which is typically 5.0 to 12V.

2) When OE is low, the chip disables its outputs, setting OUTA/OUTC high and OUTB/OUTD low. This condition helps to properly pre-charge the AC coupling capacitors that users can optionally add in series with the gate-driver circuit of the external P/N-channel FET pairs.

The MD1811's output stage has separate power pins that enable users to select the output signal's high and low levels independently from the supply voltages that the main part of the circuit uses. For example, the input logic levels could be 0 and 1.8V, the control logic might run from ±5.0V, and the output levels may lie anywhere in the range ±5.0V.

Typically, the MD1811's output has rise and fall times of about 6ns when driving a 1000pF load. The output stage is capable of peak currents of up to ±2.0A, depending on the system's supply voltages and load capacitance. Such high currents are necessary to drive the input capacitances of the output MOSFETs for fast switching speeds.

Both the Supertex TC6320 and TC2320 comprise N- and P-channel MOSFET pairs with low threshold voltages (2.0V maximum). These 8-Lead SOIC packaged devices feature 200V breakdown voltages, 2.0A output peak current capabilities, and low input capacitance (110pF maximum). The TC6320 integrates the gate-source resistors and Zener diodes that high voltage pulse-drivers require; the TC2320 omits these additional components.

The high output current capability of these MOSFETs speeds output rise and fall times, while their low input capacitance minimizes propagation delays. In practice, the Miller effect increases a MOSFET's effective input capacitance (C_{IN}) beyond the device's intrinsic gate capacitance (C_{ISS}), adding the reverse transfer capacitance (C_{RSS}) times the product of the device's transconductance (G_{FS}) and load resistance (R_L):

$$C_{IN} = C_{ISS} + C_{RSS} (G_{FS} * R_L)$$

As a result, the output transistors for pulser applications require low C_{RSS} and C_{ISS} values, together with high output current capabilities, low on-resistances, and high breakdown voltages.

During power up/down conditions, the high voltage supplies V_{PP} and V_{NN} can inject transient voltages greater than 20V via the output transistors' parasitic gate-to-source capacitances. The maximum permissible gate-to-source voltage (V_{GS}) is ±20V. The TC6320's integral 15-18V Zener diodes across its gate and source terminals protect against such transient voltages. But even if it's possible to slowly ramp the high voltage supplies, these Zener diodes are still crucial, as they also serve as the DC voltage restoration stage for the gates.

Note that it's possible to vary the V_{PP} and V_{NN} voltages without making significant changes to the circuit configuration. For example, V_{NN} can be 0V and V_{PP} +200V for positive unipolar pulses—see **Figure 2**. Or V_{NN} can be -200V and V_{PP} 0V for a negative unipolar pulser—see **Figure 3**.

To operate the MD1811 from a single supply rail, connect the VDD and VH pins to a supply of +5.0, +10, or +12V and connect VSS and VL to ground. The MD1811 also can also take its power from dual supply rails. If V_{DD} is +5.0 or +6.0V, then the V_{SS} and V_L negative supplies are -5.0 or -6.0V. In any case, ensure that the MD1811's GND pin connects to the system's logic ground.

For the unipolar examples where V_{PP} is 200V, the high voltage supply's bypass capacitors require working voltages greater than 200V. This observation also applies to the gate coupling capacitors. In the case of a positive unipolar output application with a single-rail supply, the OUTB to N-FET gate can dispense with the coupling capacitor and use straight forward DC coupling.

Note that the drain terminals of the two MOSFETs can be connected in certain applications, which eliminates the high voltage requirements for the diodes. But if the circuit is a multi-level pulser such as the drain of TC2320 in **Figure 1**, these drains must not be connected as the output channel diodes not only serve as isolation diodes, but also steer the positive and negative output currents.

Figure 2. MD1811 Driving a +200V Unipolar Pulser

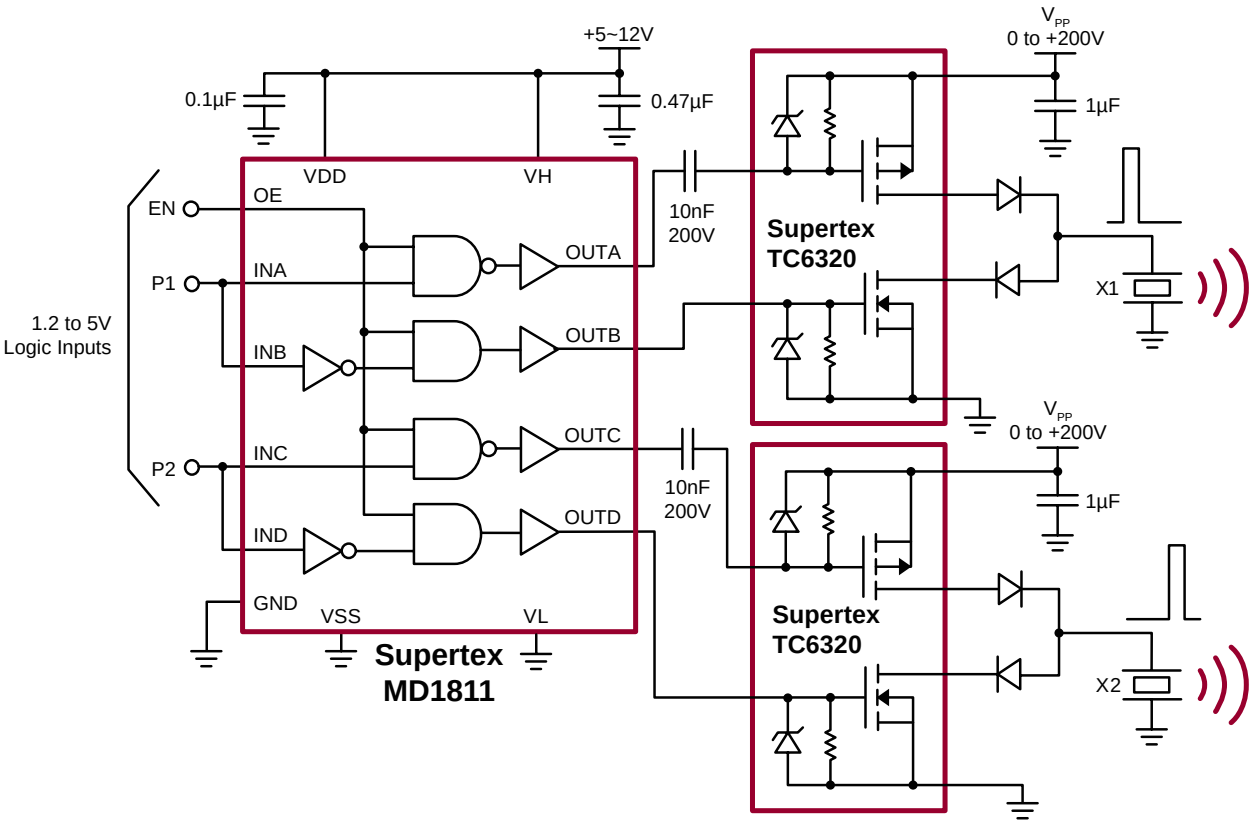
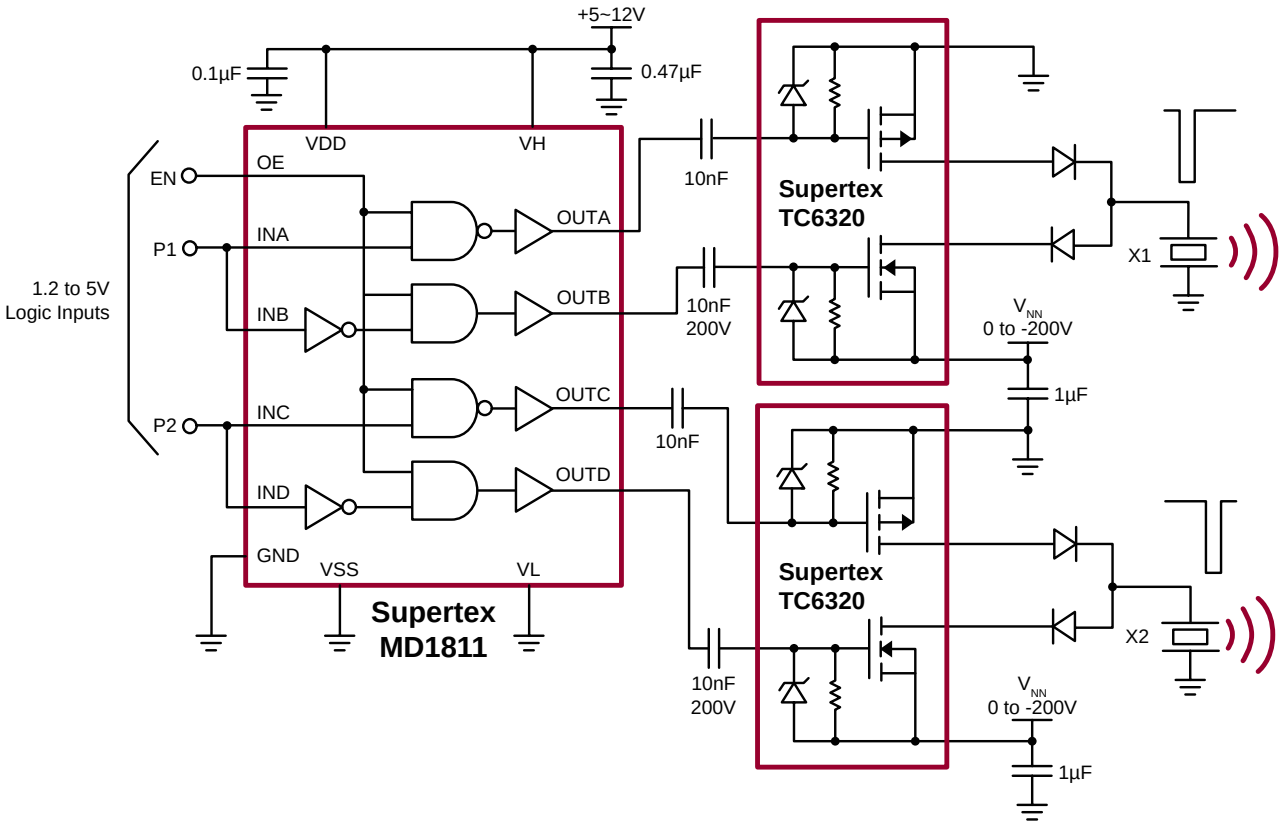


Figure 3. MD1811 Driving a -200V Unipolar Pulser



PCB Layout Design Considerations

The MD1811's high speed demands low inductance bypass capacitors to decouple its various supply pins. The GND pin is the logic-zero reference input and must connect to the system's digital ground. The INA, INB, INC, IND and OE pins are connected to logic sources with a swing from GND to a logic-high level within the range 1.2 to 5.0V.

Use high-speed PCB trace design practices that are compatible with the circuit's operating speed. The internal circuitry of the MD1811 can operate at up to 100MHz, with the primary speed limitation being due to load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors should be as close to the chip's pins as possible. Unless the load specifically requires bipolar drive, the VSS and VL pins should have low inductance feed-through connections directly to a solid ground plane. If these voltages are not zero, they will require bypass capacitors similar to the positive power supplies.

The VH and VL supplies determine the output logic levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with a low-impedance bypass capacitor at the chip's pins. A ceramic capacitor of up to 1.0µF may be appropriate. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. A common voltage source and local decoupling capacitor may be used for the VDD and VH pins, which should always have the same DC level applied to them. For applications that are sensitive to jitter and noise, insert another ferrite bead between VDD and VH and decouple each pin separately.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small value resistor in series with the output to obtain better waveform integrity at the load terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Pay particular attention to the parasitic coupling from the driver's output to the input signal terminals. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

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