Application Note

HV440 High Voltage Ring Generator

by Jimes Lei, Applications Engineering Manager

Introduction

The Supertex HV440 is used for implementing a pulse width modulated high voltage ring generator for telecommunication applications. The HV440 can operate in both closed-loop or open-loop. A closed-loop design is more complex, but provides better load regulation and lower THD compared to an open-loop design.

In this application note, a closed-loop design is discussed. The output ring voltage is 62VRMS at 20Hz with load capabilities of 5 and 20 RENs. The telephone must see a minimum of 40VRMS, otherwise ringing is not guaranteed. Ring generators are typically sinusoidal. Common ring frequencies are 20 and 25Hz. Telephone loads are rated in RENs (ring equivalent number). One North American REN is equivalent to 6930Ω in series with 8.0μF. For a given telephone line, the ring generator must be able to drive 5 RENs.

The output MOSFETs integrated in the HV440 can drive up to 5 North American RENs. For applications requiring loads greater than 5 RENs, the HV440 can also drive external Supertex MOSFETs, TP2522N8 and TN2524N8 for loads of up to 20 RENs. Complete schematics for a 5 REN and a 20 REN ring generator with their bill of materials can be found at the end of this application note.

General Circuit Description

The implementation of the ring generator circuit is very similar to that of a class D amplifier. Referring to Figure 1, a logic voltage high frequency pulse width modulated sine wave signal is generated by the sine wave reference, ramp generator, and error amp. The PWM signal is the input signal for the HV440. The HV440 will amplify the 0 to 5V signals to a negative high voltage (V_{NN1}) and a positive high voltage (V_{PP1}). The LC filter will convert the high voltage PWM signal from the HV440 to a high voltage sinusoidal waveform which is used as the ring output. A feedback path is connected to the ring generator output and is compared to the sine wave reference. Any differences between the sine wave reference and the ring generator output are corrected by adjusting the pulse widths controlled by the error amplifier. The various blocks shown in Figure 1 are discussed separately in more detail in the following sections.

Sine Wave Reference

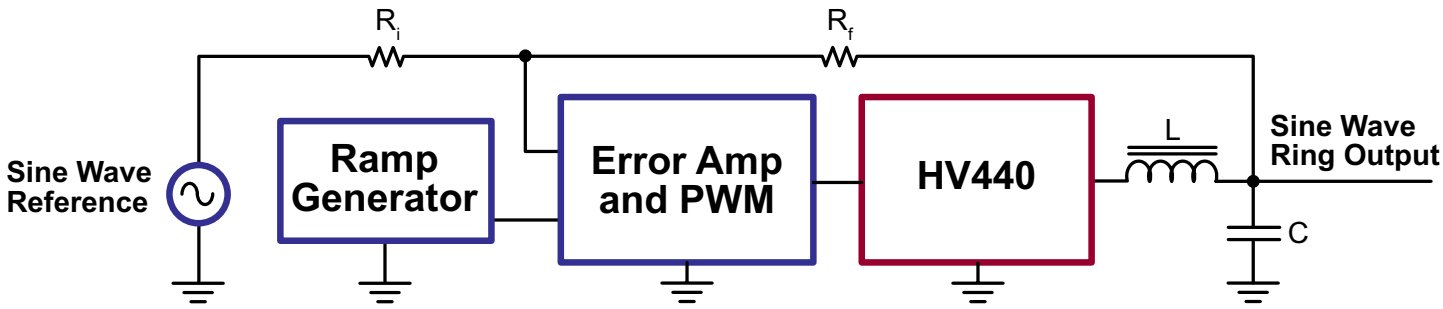
A low voltage reference sine wave signal is required to generate the output ringer signal. A wien-bridge oscillator was chosen to generate the reference sine wave as shown in Figure 2. The Wien-Bridge Oscillator was selected for its simplicity. Other ways of generating the reference sine wave are by using sine wave generator integrated circuits such as an Exar XR-2206, a Micro Linear ML2035, or a Philips PCD3311C.

However, the referenced signal is not limited to sinusoidal waveforms. Trapezoidal ringing waveform with crest factors between 1.2 to 1.6V are also acceptable. There are two main advantages to using trapezoidal waveforms over sinusoidal waveforms. They are: a) It is easier to generate, b) With a given peak-to-peak voltage, higher RMS voltages can be obtained when using crest factors of less than 1.414. The disadvantage of using trapezoidal ring generators is that sinusoidal ring generators are more widely accepted.

Three main parameters need to be considered when designing the sine wave reference. They are as follows:

1. *DC offset voltage,*
2. *Peak-to-peak amplitude, and*
3. *Ringing frequency.*

Figure 1: Conceptual Block Diagram



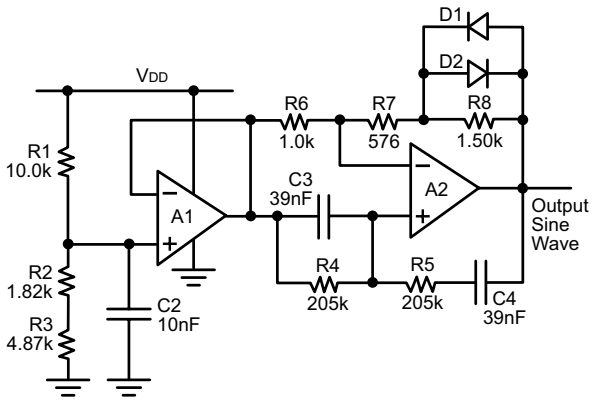


Figure 2: Wien-Bridge Oscillator

1) DC Offset Voltage

The Wien-Bridge Oscillator operates on a single 5V supply, V_{DD}. The sinusoidal signal generated by the Wien-Bridge Oscillator needs to be superimposed on a DC offset voltage set by R_1, R_2, R_3, C_2, and A_1. The DC offset voltage level should be set in such a way that it will not saturate and cause the sine wave signal to be clipped.

Op-amp A_1 is a National LM2902 which has an output voltage swing of 0V to V_{DD} -1.5V. For a V_{DD} voltage of 5V ± 5%, the worst case V_{DD} voltage would be 5V - 5% which is 4.75V. When sinking current, the voltage drop can be 0.5V. The voltage for the sine wave should therefore be in between 0.5 and 3.25V. A DC offset of 2.0V was selected. A 2.0V peak-to-peak amplitude was chosen for the sine wave. The output of A_2 will therefore swing from 1.0 to 3.0V. This leaves 0.5V margin for the low end of the sine wave and 0.25V margin for the high end of the sine wave.

R_1, R_2, and R_3 divides the V_{DD} voltage to 2.0V when V_{DD} = 5.0V. C_2 is used as a DC coupling capacitor to filter any AC noise that may be on V_{DD}. A_1 is used as a unity gain buffer to generate a low output impedance voltage reference. The DC offset voltage with the values shown in Figure 2 is:

$$DC\ offset = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \bullet V_{DD}$$

$$= \frac{1.82K\Omega + 4.87K\Omega}{10K\Omega + 1.82K\Omega + 4.87K\Omega} \bullet 5.0V$$

$$= 2.0V$$

R3 is used to generate a different DC voltage to set the output ring generator DC offset. The voltage generated by R3 is discussed in the error amplifier section.

2) Peak-to-Peak Amplitude

The amplitude is determined by the two clamping diodes D_1 and D_2. Their forward voltage drop sets the initial conditions in determining the amplitude. It should be kept in mind that in order for oscillation to occur in a Wien-Bridge circuit, the gain must be equal to or greater than 3. The gain is determined by R_6, R_7, and R_8 in the following equation:

$$Gain = 1 + \frac{R_7 + R_8}{R_6}$$

$$= 1 + \frac{576\Omega + 1.50K\Omega}{1.00K\Omega}$$

$$= 3.076$$

D_1 and D_2 are in parallel with R_8. When D_1 or D_2 are forward biased, they will be shunting R_8, thereby lowering its effective DC resistance. The DC gain of 3.076 will start to decrease. If the gain becomes less than 3, oscillation will stop. The forward voltage drop, V_f, of the D_1 and D_2 will settle to a value such that its DC resistance in parallel with R_8 will give a DC gain of 3. The output amplitude of A_2 can be approximated with the following equation:

$$V_{P\text{-}P} = 2 \bullet \frac{V_f \bullet 3K\Omega}{3K\Omega - (R6 + R7)}$$

The forward diode drop of D_1 and D_2 can be determined by evaluating its I-V curve. The curve is shown in Figure 3. The bias currents for D_1 and D_2 should be set relatively high to minimize any leakage current effects.

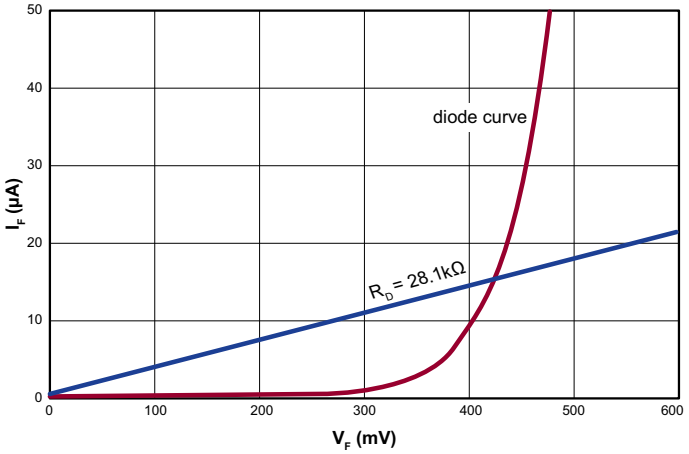


Figure 3:
Forward bias current vs.Forward Diode Voltage

For a DC gain of 3, letting RD be the DC resistance of D_1 and D_2 which are in paralllel with R_8, RD can be determined by the following calculation:

$$3 = 1 + \frac{R_7 + \frac{R_8 \cdot R_D}{R_8 + R_D}}{R6}\text{ , solving for } R_D$$

$$R_D = \frac{R_7 \cdot R_8 - 2R_6 \cdot R_8}{2R_6 - R_7 - R_8}$$

$$= \frac{(576\Omega \cdot 1.5K\Omega) - (2 \cdot 1.0K\Omega \cdot 1.5K\Omega)}{2 \cdot 1.0K\Omega - 576\Omega - 1.5K\Omega}$$

$$= 28.1K\Omega$$

Referring to the I-V curve on Figure 3, V_F is 425mV for an R_D of 28.1KΩ. The sine wave reference amplitude is therefore theoretically 1.8V peak-to-peak. The peak-to-peak voltage is expected to be slightly greater than what the theoretical values predict due to the response time of the circuit. Oscillation will not stop instantaneously once its gain is less than 3. It will be slightly less than 3. The actual value for the gain was measured to be 2.94. The measured output voltage was 1.95V peak-to-peak.

3) Ringing Frequency

The sinewave frequency is determined by R_4, R_5, C_3, and C_4. The sinewave frequency is set for 20Hz which is commonly used in North America. Different countries will require different frequencies. For example, 25Hz is commonly used in Germany. By changing the values of R_4 and R_5, different frequencies can be easily achieved. For 20Hz, 205KΩ is used for R_4 and R_5, and 39nF is used for C_3 and C_4. The calculation for the frequency is shown below.

$$freq = \frac{1}{2\pi\sqrt{R_4R_5C_3C_4}}$$

$$= \frac{1}{2 \cdot 3.14 \cdot \sqrt{205K\Omega \cdot 205K\Omega \cdot 39nF \cdot 39nF}}$$

$$= 19.9Hz$$

Ramp Generator

Figure 4 is the voltage ramp generator circuit consisting of R_9, R_{10}, R_{11}, R_{12}, R_{13}, C_5 and Comp1. The ramp frequency sets the PWM frequency of the ring generator. The PWM frequency for the 5 REN circuit is different from the 20 REN circuit to avoid output inductor saturation.

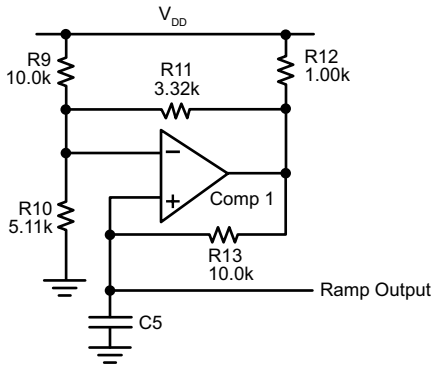


Figure 4: Voltage Ramp Generator

The ramp generator is based on a simple R-C charge and discharge circuit. The waveform does not need to be an ideal linear ramp because the overall circuit is closed loop. Any non-linearities on the ramp voltage will be taken into consideration by the error amplifier. The ramp output voltage will swing from V_{LL} to V_{UL}. Its voltage and frequency can be approximated with the following equations:

$$V_{UL} = \frac{R_{10}(R_9 + R_{11} + R_{12})}{R_9(R_{11} + R_{12}) + R_{10}(R_9 + R_{11} + R_{12})} \cdot V_{DD}$$

$$V_{LL} = \frac{R_{10}R_{11}}{R_{10}R_{11} + R_9(R_{10} + R_{11})} \cdot V_{DD}$$

$$t_{DIS} = -R_{13}C_5\,ln(V_{LL} / V_{UL})$$

$$t_{CHG} = -(R_{12} + R_{13})C_5\,ln[(V_{UL} - V_{FINAL})/(V_{LL} - V_{FINAL})]$$

$$V_{FINAL} = (V_{DD} - V_{UL})\,[R_{11} / (R_{11} + R_{12})] + V_{UL}$$

$$f = 1 / (t_{CHG} + t_{DIS})$$

where,

V_{DD}	=	5.0V supply
V_{UL}	=	Upper limit
V_{LL}	=	Lower limit
t_{DIS}	=	Discharge time
t_{CHG}	=	Charge time
V_{FINAL}	=	Final charge value
f	=	Ramp frequency

Using the values shown in Figure 4:

For 5 REN circuit, C_5 = 680pF	For 20 REN circuit, C_5 = 330pF
V_{UL} = 3.14V	V_{UL} = 3.14V
V_{LL} = 0.84V	V_{LL} = 0.84V
V_{FINAL} = 4.57V	V_{FINAL} = 4.57V
t_{DIS} = 8.97µs	t_{DIS} = 4.35µs
t_{CHG} = 7.17µs	t_{CHG} = 3.48µs
f = 62kHz	f = 128kHz

The voltage ramp generator will have a typical voltage swing of 0.84 to 3.14V at a frequency of 62kHz for the 5 REN circuit and 128kHz for the 20 REN circuit. The voltage swings are well within the operating input voltage range of comparators and output voltage swing of the op amps.

Error Amplifier / PWM

Pulse width modulated (PWM) signals need to be generated as the input signals for the Supertex HV440. This is accomplished by using op amp A_3 and comparator Comp2 as shown in Figure 5. A_3 is configured as an error amplifier. It compares the desired output ringing voltage with the reference sine wave generated from op amp A_2. The output of A_3 is compared to the ramp generator via comparator Comp2. The output of Comp2 is the PWM output operating at the same frequency as the ramp generator frequency. The PWM output duty cycle can vary from 0% to 100% controlled by the output of the error amplifier, A_3. As the output of A_3 increases, the duty cycle also increases.

R_{14} and R_{15} set the overall gain for the circuit. The DC offset for the output ringer voltage is determined by setting the appropriate voltage on C_1 via resistor divider R_1, R_2, and R_3. The circuit in Figure 5 is set for a nominal output voltage of $62V_{RMS}$ and a DC offset of -48V. The following equations can be used to set the output RMS voltage and DC offset:

$$Reference\ Sine\ Wave = 2.0VDC + 0.69V_{RMS}$$

$$DC\ offset = 2.0V \bullet \frac{-R_{15}}{R_{14}} + V_{DD} \bullet \frac{R_3}{R_1 + R_2 + R_3} \bullet (1 + \frac{R_{15}}{R_{14}})$$

$$Output_{RMS} = 0.69\ (\frac{R_{15}}{R_{14}})$$

C_6 and R_{16} set the cutoff frequency for A_3. If the cutoff frequency is too high, it will amplify noise, whereas if it is too low, it will cause output distortion. The frequency should be much greater than the ringing frequency and much lower than the PWM frequency. C_6 and R_{16} are set at 1.6kHz.

Supertex HV440

The block diagram for the Supertex HV440 is shown in Figure 6. It operates from a positive high voltage supply, V_{PP1}, a negative high voltage supply, V_{NN1}, and a low voltage supply V_{DD}. Maximum operating differential voltage (V_{PP1}-V_{NN1}) is 220V. The V_{DD} supply is designed for 5V ± 5%. Circuit operation for the following sections are described:

1. *Logic block,*
2. *Linear regulators,*
3. *Current sense, and*
4. *Output MOSFET/gate driver.*

Figure 5: Error Amplifier/PWM

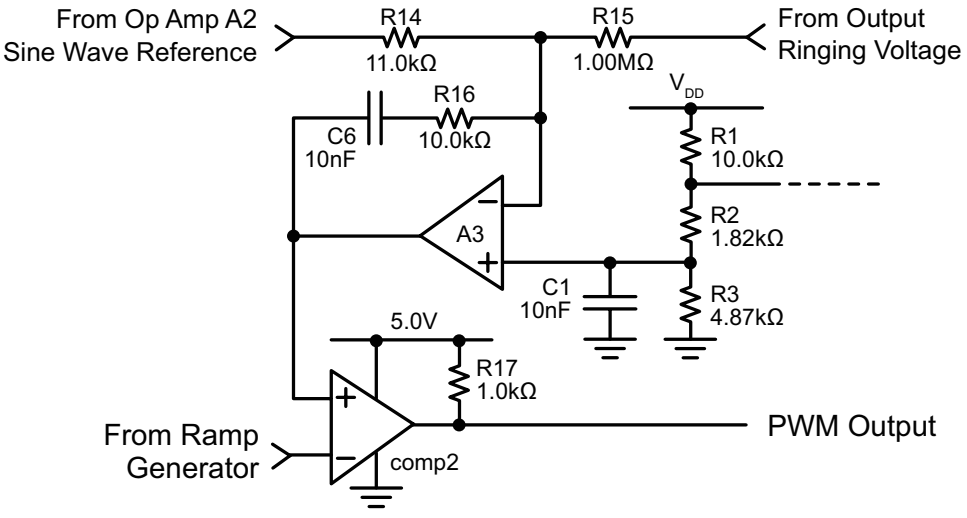
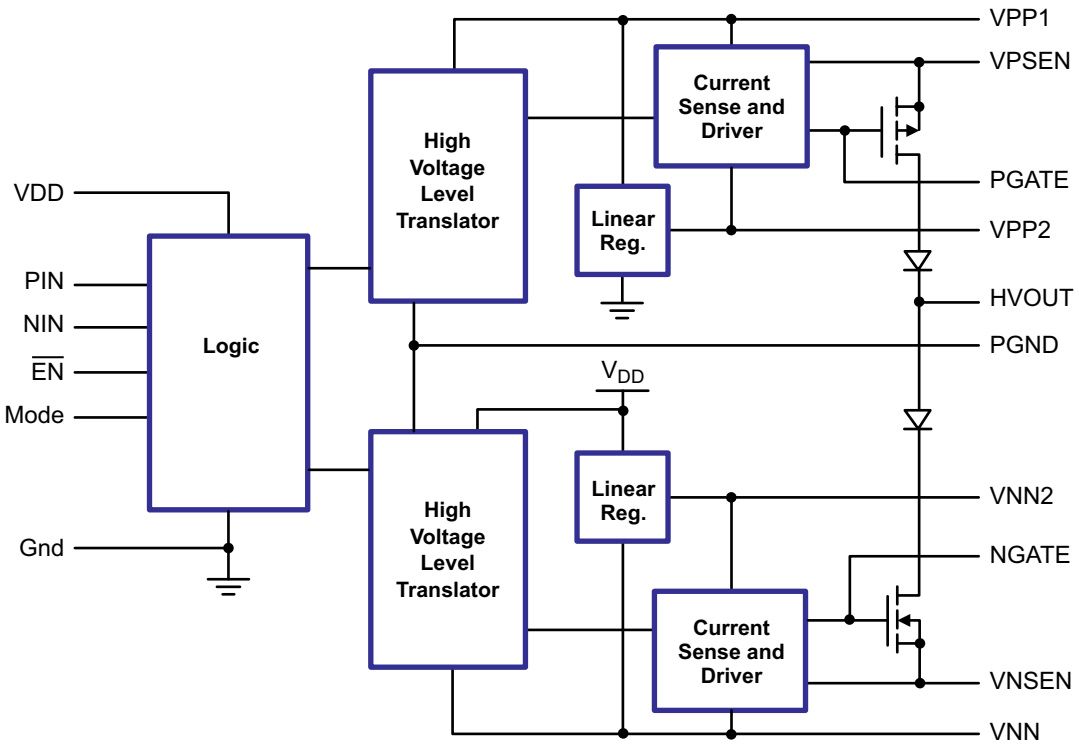


Figure 6: HV440 Detail Block Diagram



1) Logic Block

The HV440 can be used in 2 different modes: 1) Single input, or 2) Dual input. In the single input mode, the N_{IN} pin is used. A logic high on N_{IN} will turn on the P-channel MOSFET pulling the output to V_{PP1}. A logic low on N_{IN} will turn on the output N-channel MOSFET pulling the output to V_{NN1}. The HV440 has a built in maximum deadband of 200ns to ensure no crossover conduction on the output. In this mode, the output is going to be V_{PP1} or V_{NN1}. In the dual input mode, the output P-channel and N-channel MOSFETs can be controlled independently via inputs P_{IN} and N_{IN}. The logic truth table is shown on Figure 7. In this application note, the single input mode is used.

Figure 7: Logic Truth Table

Logic Inputs				Outputs		
N_{IN}	P_{IN}	Mode	EN	V_{PGATE}	V_{NGATE}	H_{VOUT}
L	L	H	L	V_{PP2}	V_{NN1}	V_{PP1}
L	H	H	L	V_{PP1}	V_{NN1}	High Z
H*	L*	H	L	V_{PP2}	V_{NN2}	*
H	H	H	L	V_{PP1}	V_{NN2}	V_{NN1}
L	X	L	L	V_{PP1}	V_{NN2}	V_{NN1}
H	X	L	L	V_{PP2}	V_{NN1}	V_{PP1}
X	X	X	H	V_{PP1}	V_{NN1}	High Z

** Turns on both P-Channel and N-Channel MOSFETs. Will shunt V_{PP1} to V_{NN1}.*

2) Linear Regulators

The HV440 has two high voltage linear regulators which generate voltages V_{PP2} and V_{NN2}. V_{PP2} is typically 16V below V_{PP1}. V_{NN2} is typically 10V above V_{NN1}. V_{PP2} and V_{NN2} will track the high voltage supplies V_{PP1} and V_{NN1}. These are generated to provide proper gate-to-source turn on voltages for the internal and external MOSFETs. Discrete MOSFETs typically have gate-to-source voltage ratings of ±20V maximum. A low voltage capacitor of 0.1µF is recommended to provide the peak currents required during the switching transition.

3) Current Sense

The current sense pins P_{SENSE} and N_{SENSE} are cycle by cycle current sense. They are independent of each other. The voltage trip point is set at a nominal voltage of 1.0V. Different sense resistor values can be selected to set the maximum allowable peak currents. This protects the device and the output MOSFETs from damage during a fault short circuit condition. The current sense is reset on the rising edge of the next clock cycle.

4) Output MOSFETs and Gate Drivers

The internal output MOSFETs in the HV440 can drive up to 5 RENs. The diodes in series with the internal MOSFETs are to prevent current from flowing the opposite direction. For loads greater than 5 RENs, external MOSFETs can be used. The gate driver, P_{GATE} and N_{GATE}, on the HV440 is designed to drive external Supertex MOSFETs TP2522N8 and TN2524N8 for load requirements of up to 20 RENs. When using external MOSFETs, the internal MOSFETs can be left unconnected by leaving HV_{OUT} unconnected.

Output

The output section for the 5 REN circuit is shown on Figure 8. A 5 REN load has an impedance of 1400Ω at 20Hz. The average peak current going to the load can be approximated by 110V/1400Ω = 79mA. A large inductance value for L_1 is desirable to keep the PWM switching frequency low to minimize switching losses. The inductor current should be kept as low as possible but no less than 79mA. The inductor, L_1, was selected based on the largest standard value available with a 79mA rating or higher in a reasonably small package. L1 was selected to be a 10mH, 120mA inductor. The peak current for the inductor can be approximated with the following equation:

$$I_{PEAK} = \frac{V_{PP1} - V_{NN1}}{2 \bullet L_1 \bullet f}$$

where,

V_{PP1} = *Positive high voltage supply*
V_{NN1} = *Negative high voltage supply*
L_1 = *10mH inductor*
f = *PWM frequency*

R_{18} and R_{19} set the current limit going through L_1. The nominal voltage sense across the sense resistor is 1.0V. A 3.9Ω sense resistor was selected for a current limit of 256mA.

Capacitor C_9 was selected such that the LC resonant frequency is at least ten times greater than the ringing frequency and ten times lower than the PWM frequency. A 0.22µF capacitor was chosen for C_9 for a resonant frequency of 3.4kHz.

Figure 9 is the output section for the 20 REN circuit. The components are selected in a similar manner as described in the 5 REN circuit. Transistors TP2522N8 and TN2524N8 are used for Q_1 and Q_2 to accommodate for the higher REN load requirement. The internal transistors in the HV440 are not used. The HV_{OUT} pin is therefore left unconnected.

Figure 8: Negative Supply

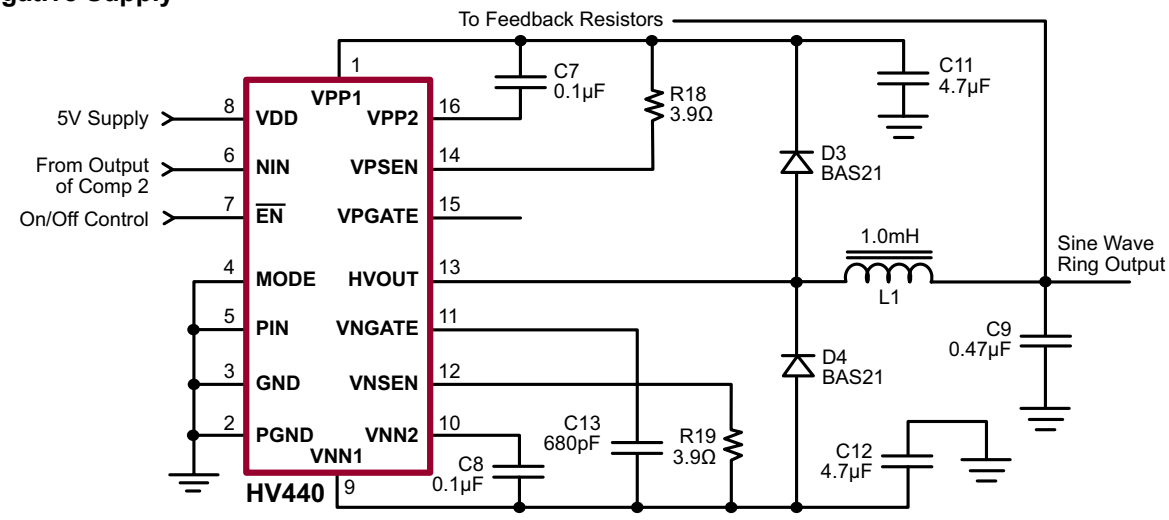
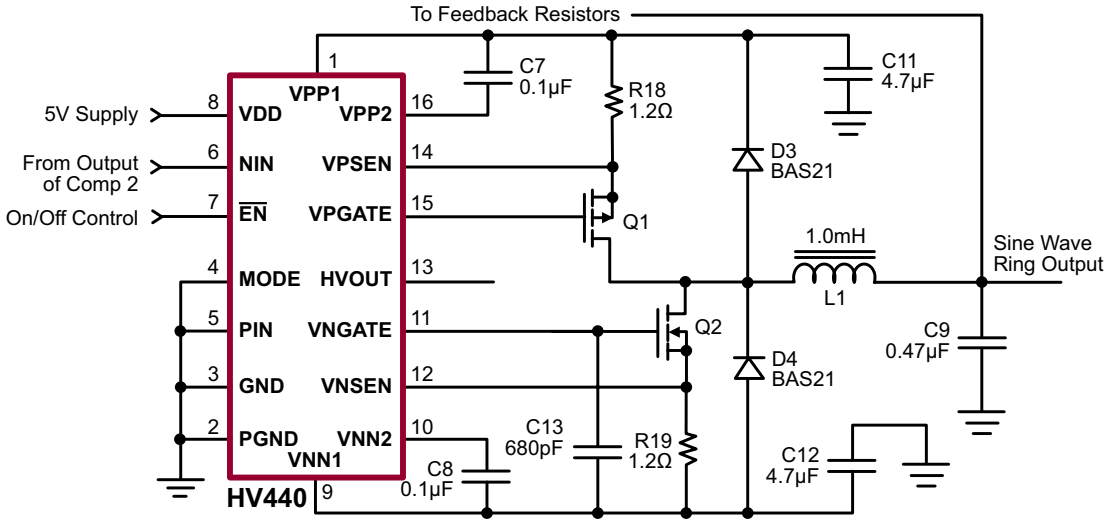


Figure 9: HV440 Output LC Filter for 20 REN



Lab test Results

The ramp generator, sine wave reference, and output ring voltage are shown on Figures 10 and 11 for the 5 REN circuit.

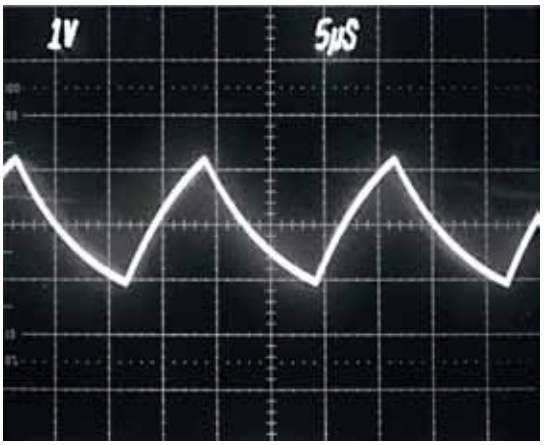


Figure 10: Ramp Output

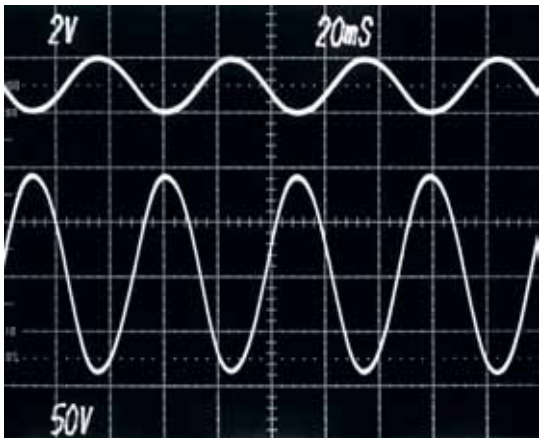


Figure 11: Ringer Output

The ramp generator, sine wave reference, and output ring voltage are shown on Figures 12 and 13 for the 20 REN circuit.

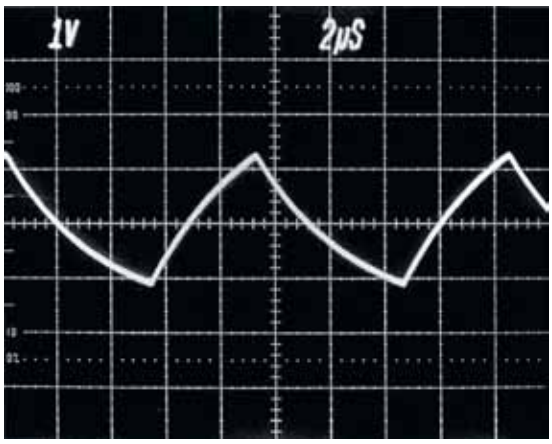


Figure 12: Ramp Output

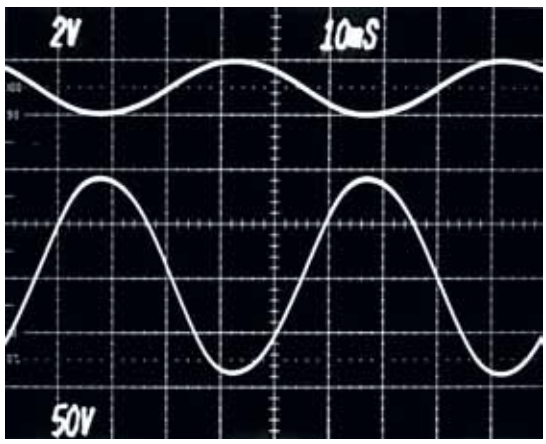
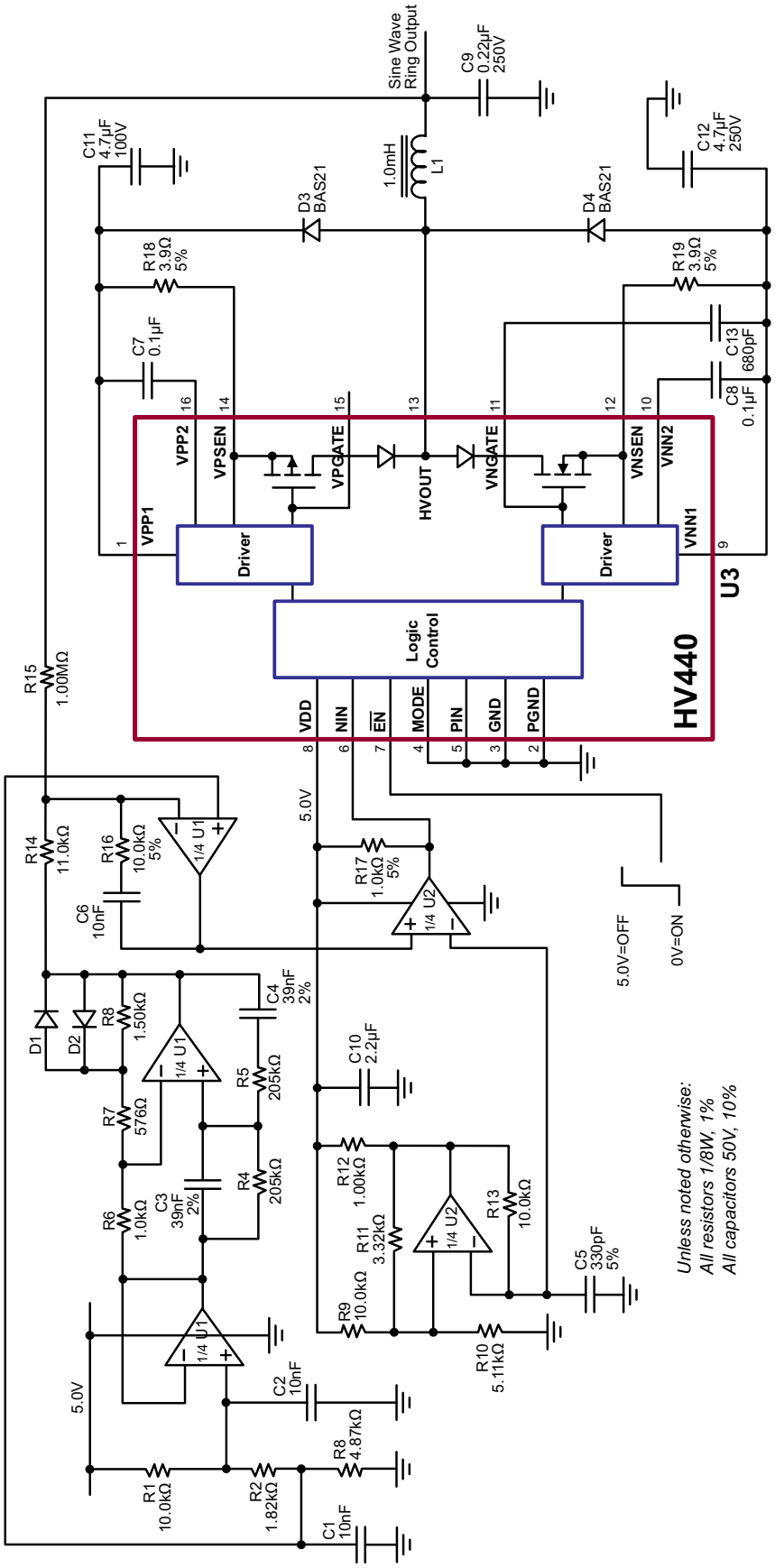


Figure 13: Ringer Output

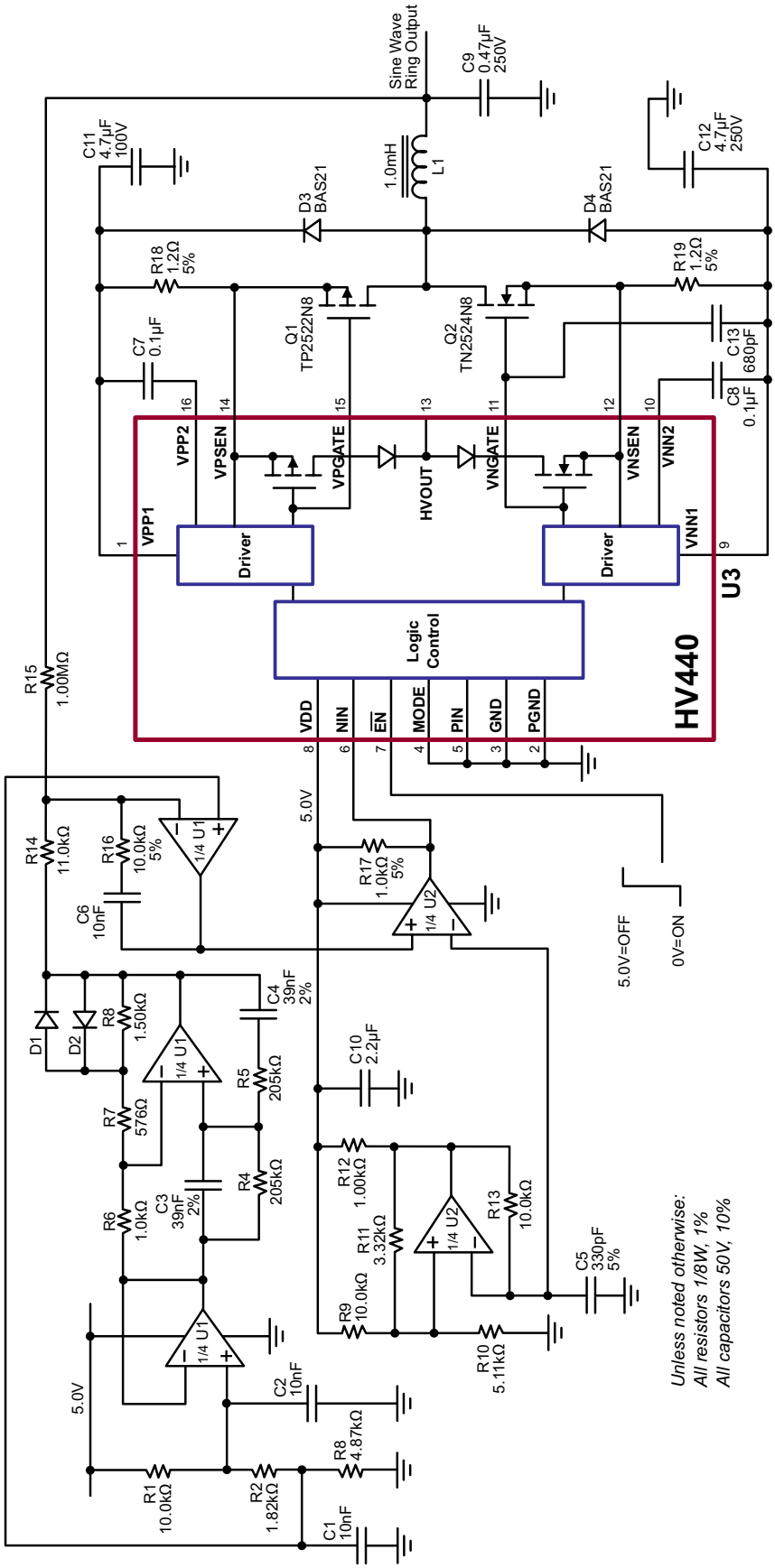
Figure 14: HV440 5 REN Ring Generator



HV440: 5 REN Ring Generator Bill of Materials

Desig	Description	Value	Tol	Rating
R1	Thick film chip resistor	10.0KΩ	1%	1/8W
R2	Thick film chip resistor	1.82KΩ	1%	1/8W
R3	Thick film chip resistor	4.87KΩ	1%	1/8W
R4, R5	Thick film chip resistor	205KΩ	1%	1/8W
R6	Thick film chip resistor	1.00KΩ	1%	1/8W
R7	Thick film chip resistor	576Ω	1%	1/8W
R8	Thick film chip resistor	1.50KΩ	1%	1/8W
R9	Thick film chip resistor	10.0KΩ	1%	1/8W
R10	Thick film chip resistor	5.11KΩ	1%	1/8W
R11	Thick film chip resistor	3.32KΩ	1%	1/8W
R12	Thick film chip resistor	1.00KΩ	1%	1/8W
R13	Thick film chip resistor	10.0KΩ	1%	1/8W
R14	Thick film chip resistor	11.0KΩ	1%	1/8W
R15	Thick film chip resistor	1.0MΩ	1%	1/8W
R16	Thick film chip resistor	10.0KΩ	5%	1/8W
R17	Thick film chip resistor	1.00KΩ	5%	1/8W
R18, R19	Thick film chip resistor	3.90Ω	5%	1/8W
C1, C2	X7R ceramic chip capacitor	10nF	10%	50V
C3, C4	Surface mount film capacitor	39nF	2%	50V
C5	Metalized polyester film capacitor	680pF	5%	50V
C6	X7R ceramic chip capacitor	10nF	10%	50V
C7, C8	X7R ceramic chip capacitor	0.10µF	10%	50V
C9	Metalized polyester film capacitor	0.22µF	10%	250V
C10	Tantalum electrolytic chip capacitor	2.20µF	20%	10V
C11	Aluminum electrolytic capacitor	4.70µF	20%	100V
C12	Aluminum electrolytic capacitor	4.70µF	20%	250V
C13	X7R ceramic chip capacitor	680pF	10%	50V
L1	Inductor	10mH	15%	120mA
D1-D2	Diode array, fast recovery	BAV99	-	70V
D3	Diode, fast recovery	BAS21	-	250V
D4	Diode, fast recovery	BAS21	-	250V
U1	Quad operational amplifier IC	LM2902M	-	-
U2	Dual high speed comparator IC	LM2903M	-	-
U3	High voltage ring generator IC	HV440WG-G	-	-

Figure 15: HV440 20 REN Ring Generator



HV440: 20 REN Ring Generator Bill of Materials

Desig	Description	Value	Tol	Rating
R1	Thick film chip resistor	10.0KΩ	1%	1/8W
R2	Thick film chip resistor	1.82KΩ	1%	1/8W
R3	Thick film chip resistor	4.87KΩ	1%	1/8W
R4, R5	Thick film chip resistor	205KΩ	1%	1/8W
R6	Thick film chip resistor	1.00KΩ	1%	1/8W
R7	Thick film chip resistor	576Ω	1%	1/8W
R8	Thick film chip resistor	1.50KΩ	1%	1/8W
R9	Thick film chip resistor	10.0KΩ	1%	1/8W
R10	Thick film chip resistor	5.11KΩ	1%	1/8W
R11	Thick film chip resistor	3.32KΩ	1%	1/8W
R12	Thick film chip resistor	1.00KΩ	1%	1/8W
R13	Thick film chip resistor	10.0KΩ	1%	1/8W
R14	Thick film chip resistor	11.0KΩ	1%	1/8W
R15	Thick film chip resistor	1.0MΩ	1%	1/8W
R16	Thick film chip resistor	10.0KΩ	5%	1/8W
R17	Thick film chip resistor	1.00KΩ	5%	1/8W
R18, R19	Thick film chip resistor	1.20Ω	5%	1/8W
C1, C2	X7R ceramic chip capacitor	10nF	10%	50V
C3, C4	Surface mount film capacitor	39nF	2%	50V
C5	NPO ceramic capacitor	330pF	5%	50V
C6	X7R ceramic chip capacitor	10nF	10%	50V
C7, C8	X7R ceramic chip capacitor	0.10µF	10%	50V
C9	Metalized polyester film capacitor	0.47µF	10%	250V
C10	Tantalum electrolytic chip capacitor	2.20µF	20%	10V
C11	Aluminum electrolytic capacitor	4.70µF	20%	100V
C12	Aluminum electrolytic capacitor	4.70µF	20%	250V
C13	X7R ceramic chip capacitor	680pF	10%	50V
L1	Inductor	1.0mH	10%	510mA
D1-D2	Diode array, fast recovery	BAV99	-	70V
D3, D4	Diode, fast recovery	BAS21	-	250V
Q1	P-Channel MOSFET	TP2522N8-G	-	220V
Q2	N-Channel MOSFET	TN2524N8-G	-	240V
U1	Quad operational amplifier IC	LM2902M	-	-
U2	Dual high speed comparator IC	LM2903M	-	-
U3	High voltage ring generator IC	HV440WG-G	-	-

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