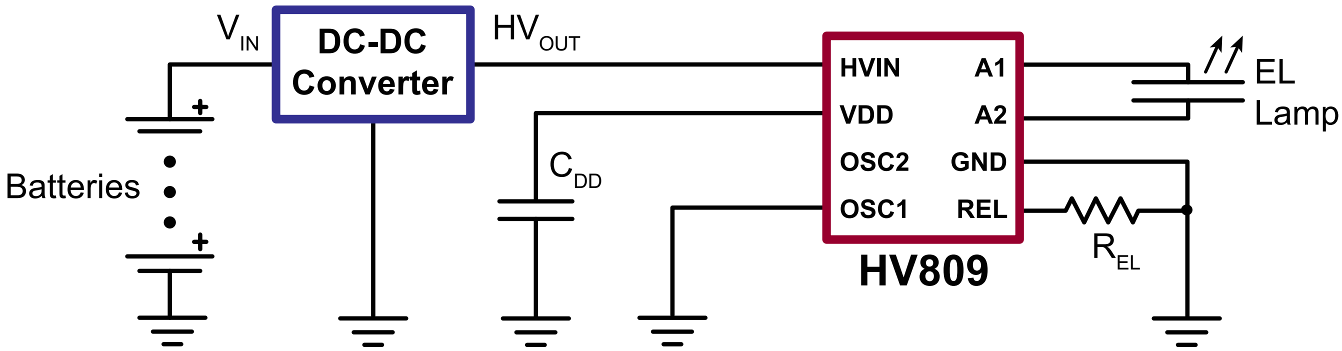
HV809 EL Lamp Driver for Battery Powered and Off-line Equipment

by Scott Lynch, Senior Applications Engineer

Figure 1: HV809 for Portable Applications



Introduction

The Supertex HV809 is designed to drive large lamps at high brightness. It can operate from a rectified/filtered 120V AC power line or from any DC source in the range of 50 to 200V. For use in battery powered applications, an external DC-DC converter is required.

This application note is divided into two sections, portable applications and off-line applications. Section I describes the operation of the Supertex's HV809 EL lamp driver for a battery operated (4 AA cells) application to drive a 12.5in^2 EL lamp to a brightness of 15ft-lm. Details are provided for designing a high voltage output DC-DC converter. Applications can be for PDA's, GPS's, hand held computers, and other portable devices requiring high brightness EL backlighting. Section II describes the HV809 operating from a 120V AC line to drive a 100in^2 EL lamp to a brightness of 20ft-lm. Applications can be signage, courtesy lighting, and accent lighting.

Section I - Portable Applications

The basic circuit configuration is shown in Figure 1. There are many different implementations in designing the DC-DC converter. In this design, an inexpensive 555 timer IC was used for the DC-DC converter. Details of the converter are discussed in a later section.

Lamp Driver Circuit and Operation

The Supertex HV809 is capable of driving EL lamps of up to 350nF at 400Hz. Input supply can be any DC voltage source from 50 to 200V. The HV809 supplies the EL lamp with an AC square wave with a peak-to-peak voltage of two times the input DC voltage.

The HV809 incorporates a lamp drive oscillator with frequency controlled by a single resistor, $R_{EL\text{-}osc}$. The oscillator controls the lamp driver output section, which consists of 4 transistors arranged in a full bridge configuration as shown in Figure 2.

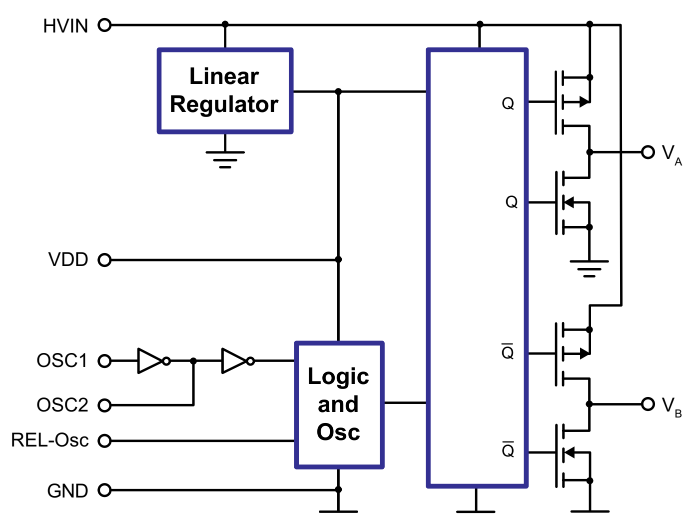


Figure 2: HV809 Lamp Driver

The supply voltage can be supplied by a rectified/filtered AC line or by an external high voltage power supply. Alternate sets of output transistors are turned on by the drive oscillator, providing a lamp drive waveform as shown in Figure 3. This design has excellent drive capability and provides a symmetrical bipolar drive, resulting in a zero-bias signal. Many lamp manufacturers recommend a zero-bias drive signal to avoid potential migration problems, thereby increasing lamp life.

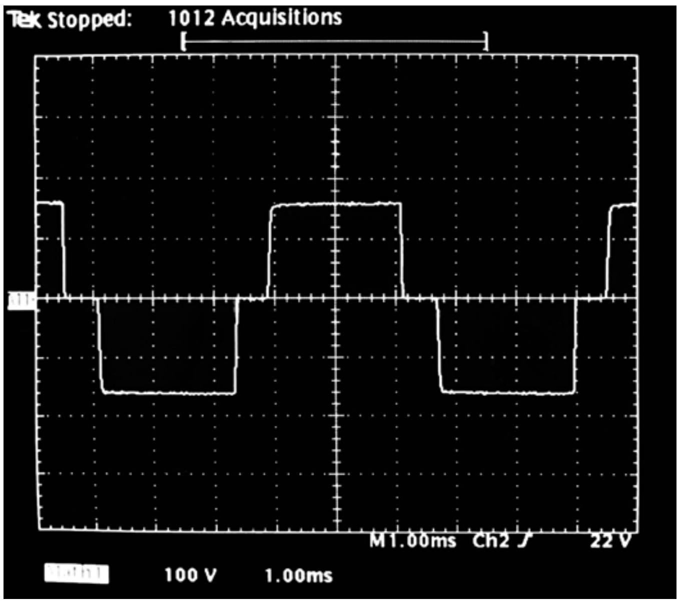


Figure 3: Lamp Drive Waveform

The design of the lamp driver section primarily consists of selecting a lamp drive frequency and voltage. Lamp frequency is controlled by $R_{EL\text{-}OSC}$. Typical values range from 510 to 5.1MΩ, with higher values yielding lower frequencies. Lamp drive voltage is determined by the high voltage supply (HV_{OUT}).

Approximately a third of the power used by the lamp driver is dissipated in the lamp resistance, and two thirds is dissipated in the HV809's bridge transistors during output transitions. With high lamp drive frequencies, large lamps, or high lamp voltages, power dissipation in the HV809 will rise. This will be a limiting factor when using the HV809 in the SO-8 package, since power dissipation cannot exceed the package rating of 500mW. The TO-220 package is rated at 15 Watts.

Figures 4 and 5 show typical characteristics for a 12.5in^2 lamp at two lamp drive frequencies. These graphs were derived from a particular lamp and characteristics will vary with other lamps.

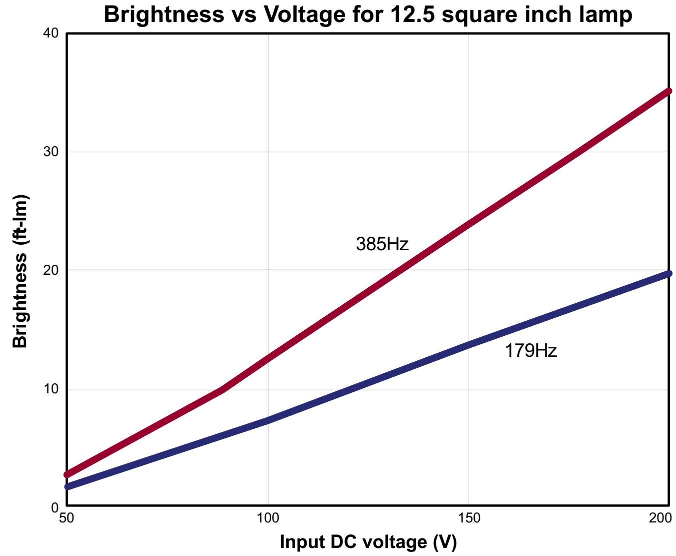


Figure 4: Lamp Brightness for 12.5in^2 Lamp

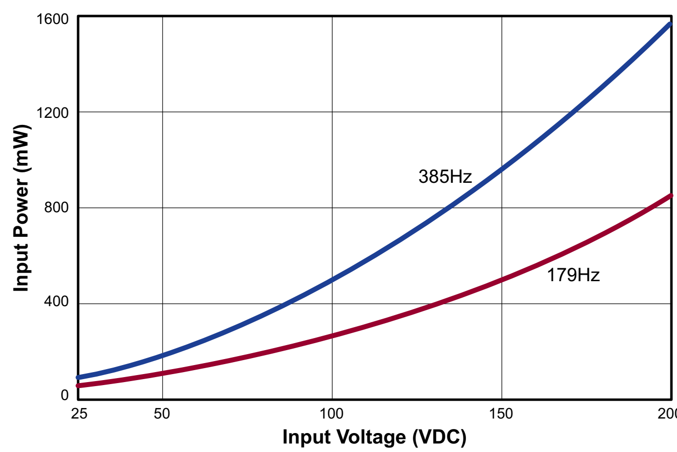
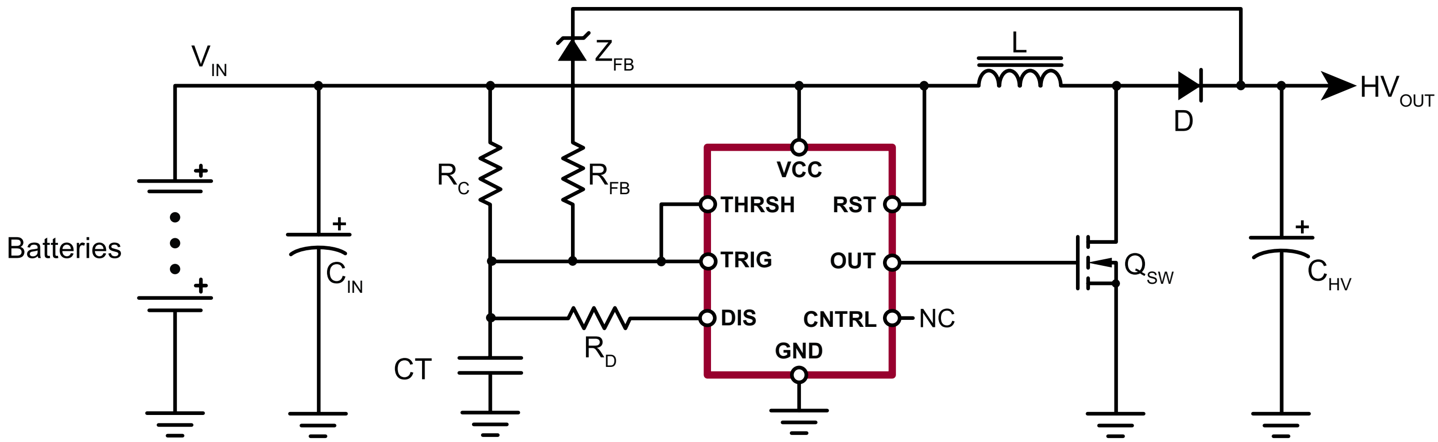


Figure 5: Input Power for 12.5in^2 Lamp

Figure 6: DC–DC Converter



Battery–Powered DC-DC Converter

An inexpensive, regulated switchmode power supply can be constructed using a 555 timer IC as shown in Figure 6. The circuit is a basic flyback boost converter using a 555 timer to provide a PWM signal to control switch Q_{SW}. By varying the duty cycle of the switch, output power can be controlled. Normally, timing components R_C, R_D, and C_T determine frequency and duty cycle. In this circuit, feedback resistor R_{FB} and Zener Z_{FB} add a positive bias to the timing circuit, with bias voltage increasing with increasing output voltage. This bias speeds up charging of timing capacitor C_T but slows down discharging, with the net result a decrease in duty cycle as output voltage increases. This mechanism provides the negative feedback necessary for regulation. With properly chosen components, this circuit regulates output voltage while maintaining a reasonably constant switching frequency.

Design of the converter consists of the following steps:

1. *Establish requirements*
2. *Determine basic converter parameters of frequency, duty cycle, and inductance (L)*
3. *Select switching transistor and rectifier (Q_{SW} and D)*
4. *Select input and output capacitors (C_{IN} and C_{HV})*
5. *Select timing components (R_C, R_D, and C_T)*
6. *Select feedback components (R_{FB} and Z_{FB})*

Establish Requirements

When designing a DC-DC converter for the HV809, three parameters are of primary importance: input voltage range ($V_{INmin/max}$), output voltage (HV_{OUT}), and output power (P_{HV}). V_{IN} is given, but HV_{OUT} and P_{HV} must be determined. If the desired lamp frequency and voltage are known, the power consumed by charging and discharging the lamp's capacitance can be estimated by the following equation:

$$P_{LAMP} = \frac{1}{2} f_{LAMP} \cdot C_{LAMP} \cdot V^2_{LAMP} \qquad (1)$$

where: f_{LAMP} = *lamp frequency*
C_{LAMP} = *lamp capacitance*
V_{LAMP} = *peak-to-peak lamp voltage*

While this equation provides a general approximation of required power, it does not account for power loss due to lamp and driver resistances. When establishing DC-DC converter requirements, it is better to determine HV_{OUT} and P_{HV} empirically. Construct an HV809 lamp driver circuit using the intended lamp. Use a high voltage bench supply to power the driver. Vary the input voltage and lamp frequency until desired lamp brightness, color, and power consumption are obtained. Measure the input voltage and current, and use these numbers as the design requirements for the DC-DC converter. If practical, make input current measurements using several lamps and driver components to get a better idea of maximum power requirements. Be sure to design to a higher power level than is actually required to allow for component tolerances and converter efficiency. Designing to at least 125% of required power is usually adequate.

Determine Operating Frequency, Duty Cycle, and Inductor

The next step is to establish the basic operating parameters of the switching converter - frequency, duty cycle, and inductance. Neglecting switch resistance, inductor losses, and other parasitics, the relationship between these parameters can be approximated by the following equation:

$$P_{HV} = \frac{(D \bullet V_{IN})^2}{2 \bullet f_C \bullet L} \quad (2)$$

where: P_{HV} = *output power*
D = *duty cycle*
V_{IN} = *supply voltage*
f_C = *converter frequency*
L = *inductor value*

Selection of a converter frequency is a good place to start, since many applications require certain converter frequencies for EMI reasons. Higher switching frequencies allow the use of smaller inductors, but lead to higher switching losses. Conversely, lower frequencies can reduce switching losses but require larger inductors. Converter frequencies in the range of 20 - 100kHz are generally suitable.

After the converter frequency has been chosen, the next step is to select an inductor. For a given switching frequency, a larger value inductor will result in lower peak currents, but may require an unreasonably high duty cycle. Duty cycle is calculated as follows:

$$D = \frac{\sqrt{2f_C L P_{HV}}}{V_{IN}} \quad (3)$$

Note that this equation can yield duty cycles greater than 100%, an obvious indication that the inductor value is too high. For the most efficient operation of the converter, duty cycle should be approximately 70% at minimum input voltage. Greater converter efficiencies occur with higher duty cycles.

For purposes of inductor rating, peak inductor current can be approximated using the following equation:

$$I_{L(PK)} = \sqrt{\frac{2P_{HV}}{f_C L}} \quad (4)$$

Selecting an inductor may require several iterations of Equations 3 and 4 to arrive at reasonable values of duty cycle, inductor value, and inductor rating. If a reasonable balance cannot be attained, converter frequency may need to be changed.

Select Q_{SW} and D

For switching transistor Q_{SW}, the most important parameters are breakdown voltage, on resistance, peak current, and power dissipation. For the rectifier, the important parameters are reverse breakdown voltage, peak repetitive forward current, average forward current, and reverse recovery time.

Since peak inductor current also flows through the switch and rectifier, it may be used to rate these components as well:

$$I_{SW(pk)} = I_{D(pk)} = I_{L(pk)} \quad (5)$$

The average rectifier current is simply the current required by the lamp driver as established in step one. Use a fast recovery rectifier (<100ns) for maximum efficiency.

The average current thru the transistor is approximately the average input current. Maximum average current will occur at minimum input voltage.

$$I_{SW} = \frac{P_{HV}}{V_{IN}} \quad (6)$$

Average power dissipation in the switch may be estimated using the following equation. Maximum dissipation in the switch will occur at minimum input voltage.

$$P_{SW} = \frac{R_{SW}(2P_{HV})^{1.5}}{V_{IN}\sqrt{f_C L}} \quad (7)$$

where: R_{SW} = *switch on resistance*

Converter frequency has little effect on switch dissipation, since higher frequencies require smaller inductors and the $f_C L$ term remains constant.

The voltage rating of both the switch and rectifier must be greater than the output voltage.

Select C_{IN} and C_{HV}

Input capacitor C_{IN} functions as an input bypass capacitor to reduce the effective source impedance. It also reduces EMI by restricting high frequency current paths to short loops. As such, C_{IN} must be located close to the converter and have a low impedance at the converter frequency. For best performance, C_{IN} impedance should be less than 1.0Ω.

$$C_{IN} \geq \frac{1}{2\pi f_C Z_{IN}} \quad (8)$$

where: $Z_{IN} = C_{IN}$ *impedance*

Output capacitor C_{HV} stores high voltage energy and also reduces EMI by restricting high frequency current paths to short loops. Like C_{IN}, C_{HV} must be located close to the converter. The value of C_{HV} is largely dependent on the desired ripple voltage on HV_{OUT}. Generally, ripple (as a fraction of output voltage) of about 10% is adequate.

$$C_{HV} \geq \frac{I_{HV}}{ripple \cdot f_{LAMP} \cdot HV_{OUT}} \quad (9)$$

where: I_{HV} = *input current to HV809*
$ripple = V_{ripple(p\text{-}p)} / HV_{OUT}$
f_{LAMP} = *lamp frequency*

Both C_{IN} and C_{HV} should be high frequency types with low ESR.

Select Timing Components R_C, R_D, and C_T

Timing components R_C, R_D and C_T determine nominal converter frequency and maximum duty cycle. Selection of these components is an iterative process. The ratio R_C/R_D sets the maximum possible duty cycle, while R_C, R_D, and C_T together determine nominal frequency. Keep in mind that feedback reduces duty cycle from the maximum and that the converter frequency varies somewhat depending upon load and supply voltage. Under no load conditions, converter frequency becomes very low in order to maintain output voltage.

Maximum duty cycle can be determined using the graph in Figure 7. Higher values of R_C/R_D, above the steep portion of curve, result in less susceptibility of maximum duty cycle to resistor tolerances. On the other hand, lower values of R_C/R_D yield tighter regulation, as described later. An R_C/R_D ratio of 4 is usually a good compromise.

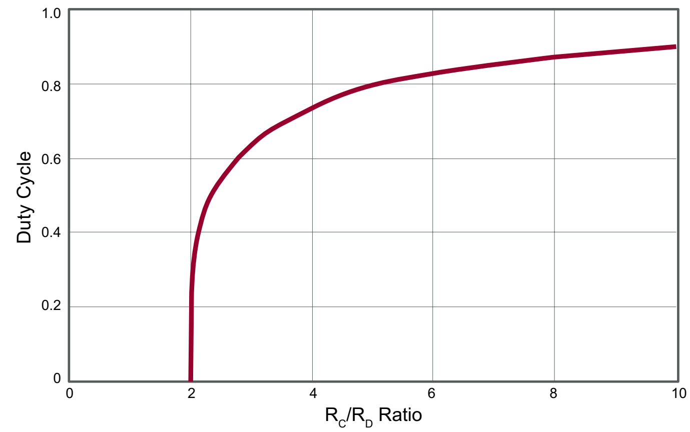


Figure 7: Maximum Duty Cycle

Maximum duty cycle may also be calculated using the following equation:

$$D_{(MAX)} = \frac{1}{1 + \dfrac{1.433}{N_{CD} + 1} \ln\left[\dfrac{1 - 2N_{CD}}{2 - N_{CD}}\right]} \quad (10)$$

where: $N_{CD} = R_C / R_D$

The R_C/R_D ratio must be greater than 2/1 for proper operation of the 555 timer. If less, timing capacitor voltage will be unable to discharge to 1/3 V_{CC} and the output of the 555 will remain low.

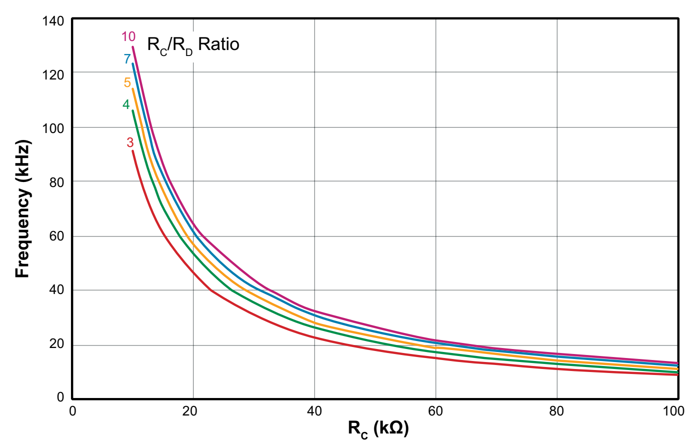


Figure 8: Nominal Converter Frequency for C_T = 1.0nf

For a given R_C/R_D ratio, nominal converter frequency can be determined using Figure 8. Converter frequency may be scaled for other values of C_T.

Alternatively, nominal converter frequency may be calculated using the following equation:

$$f_{C(NOM)} = \frac{1}{R_C C_T \left(0.693 + \frac{1}{N_{CD} + 1} \ln\left[\frac{1 - 2N_{CD}}{2 - N_{CD}}\right]\right)} \quad (11)$$

It may take several iterations to select values of R_C, R_D, and C_T to attain the frequency and duty cycle established previously.

Select Feedback Components R_{FB} & Z_{FB}

Output voltage is determined by the Zener voltage plus an amount of bias voltage needed to vary the duty cycle of the timing circuit.

$$HV_{OUT} = V_Z + V_{BIAS} \quad (12)$$

The amount of bias will vary depending on load and input voltage. The extreme limits of bias voltage are given in Equations 13 and 14. Minimum bias occurs under full design load at minimum input voltage. Maximum bias voltage occurs under no load condition at maximum input voltage. Since the HV809 presents a constant load, actual bias voltages during normal operation will be well within these limits.

$$V_{BIAS(min)} = \frac{1}{3} V_{IN} \quad (13)$$

$$V_{BIAS(MAX)} = V_{IN}\left[\frac{1}{3} - \frac{1}{1 + N_{CD} + \frac{1}{N_{FBC}}}\right]\left[1 + N_{FBC}(N_{CD} + 1)\right] \quad (14)$$

where: $N_{FBC} = R_{FB} / R_C$
$N_{CD} = R_C / R_D$

Bias voltage, as a function of R_C / R_D and R_{FB} / R_C, can be determined using Figure 9. Note that $V_{BIAS(min)}$ is independent of the resistor ratios.

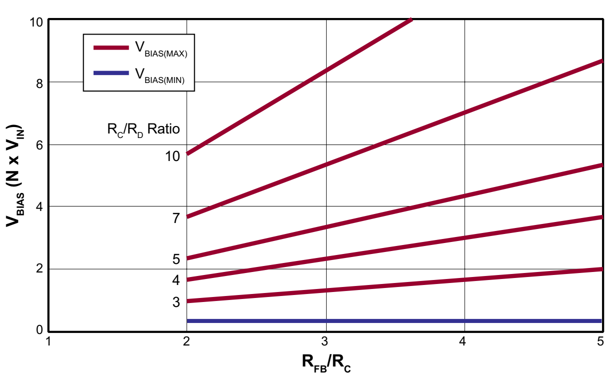


Figure 9: Bias Voltages

As can be seen from the graph, lower R_{FB} / R_C ratios yield lower bias voltages, resulting in better regulation. However, there is a lower limit on R_{FB}. The limiting condition is at start-up when the output is at zero volts and the feedback Zener is forward biased. If R_{FB} is too low, it will prevent timing capacitor voltage from rising to 2/3 V_{CC} as required for normal operation of the 555, resulting in switch Q_{SW} staying on and current rising to destructive levels. To prevent this from occurring, the ratio of R_{FB} /R_C must always be greater than two.

For best regulation, select an R_{FB} as low as possible, while keeping the R_{FB} /R_C ratio greater than two using worst-case resistor tolerances. Select the Zener voltage to be the desired output voltage, minus 1/2 the maximum bias voltage, rounding down to the next lower standard value when necessary.

Example Circuit

This section describes the design of a lamp driver circuit optimized to drive a 12.5in^2 lamp to 15ft-L brightness using 4 AA cells as the primary power source.

Requirements

To determine power requirements, an HV809 lamp driver was constructed and operated from a bench power supply. Lamp frequency was set at 200Hz for long lamp life and reasonable efficiency. An input voltage of 160V provided 15ft-L of brightness. (Note that EL lamps from various manufacturer will have different characteristics due to differences in manufacturing processes and materials used.)

Input current was measured to be 3.3mA resulting in an input power requirement of 528mW. Adding a 25% margin yields a design power level of 660mW.

Assuming 2/3 of the 528mW of input power is dissipated in the HV809, it will dissipate 352mW, well within the SO-8 package spec of 500mW.

Maximum input voltage with 4 new batteries is 6.0V. Minimum input voltage is the minimum operating voltage of the 555 timer, 4.5V.

To summarize the requirements:

V_{IN}	=	4.5 - 6.0 volts
V_{OUT}	=	160 volts
P_{HV}	=	660mW

Operating Frequency, Duty Cycle, and Inductor

A nominal converter frequency of 23kHz was chosen. This frequency is low to minimize switching losses, yet is outside the audible range to minimize any potential noise.

Next, several standard values of inductors were tried. Using Equation 3, duty cycle was calculated for each inductor value over the input voltage range of 4.5 - 6.0 volts. Peak inductor current was also calculated using Equation 4. The design power level of 660mW was used.

L (µH)	D (%)	$I_{L(pk)}$ (mA)
220	43–57	510
330	53–70	420
470	63–84	350

The duty cycle for the 330µH inductor at minimum input voltage (70%) best fits the recommended 70% duty cycle. A J. W. Miller PM105-331K, 330µH, 1.15Ω, surface mount inductor with a current rating of 520mA was chosen.

Q_{SW} and D

For the diode, a BAV21W meets all of the requirements.

Characteristic	Required	BAV21W
Reverse breakdown voltage	>160V	200V
Peak repetitive current	>420mA	625mA
Average forward current	>3.3mA	200mA
Reverse recovery time	<100ns	50ns

For the switch, a Supertex VN2224N3 MOSFET was selected.

Characteristic	Required	VN2224N3
Breakdown voltage	>160V	240V
Peak current	>420mA	7.0A
Average current	>147mA	900mA
On resistance	-	1.25Ω
Power dissipation	>153mW	1.0W

Average switch current was calculated using Equation 6. Power dissipation for the switch was calculated using Equation 7.

C_{IN} and C_{HV}

For the nominal converter frequency of 23kHz and a desired C_{IN} impedance of less than 1.0Ω, Equation 8 calculates that C_{IN} must be greater than 6.9µF. The next higher standard value of 10µF is selected.

For the 200Hz lamp frequency, a ripple factor of 10%, and the previously measured HV809 input current of 3.3mA, Equation 9 calculates that C_{HV} should be at least 1.0µF. Since this is a standard value, 1.0µF is used.

Timing Components R_C, R_D, and C_T

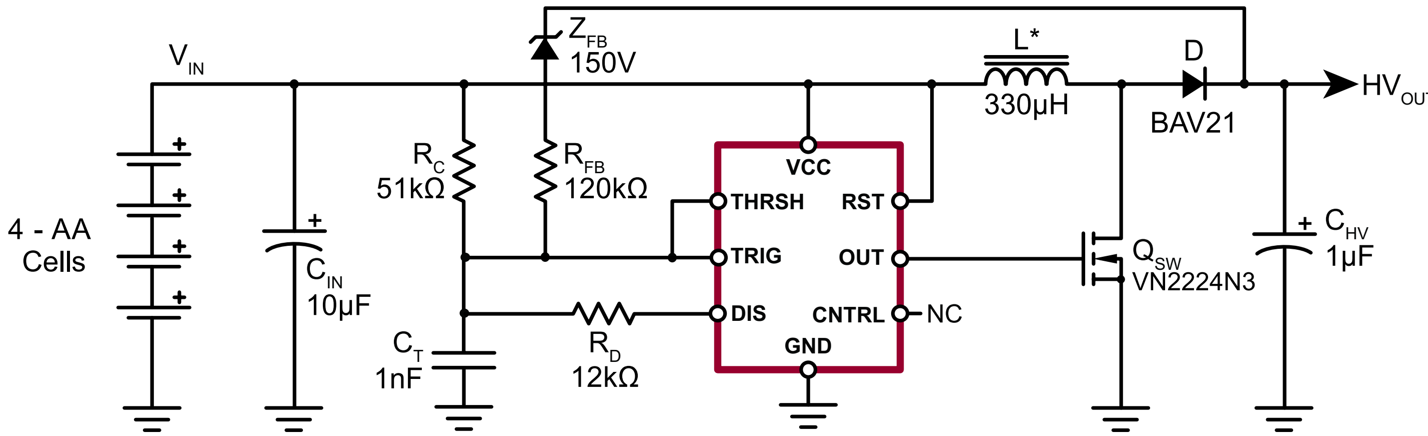
As determined in step 2, maximum duty cycle is 70% at 4.5 volts. Using Figure 7, a 70% duty cycle corresponds to an R_C / R_D ratio of 3.5. Adding some margin for resistor tolerances, a target ratio of 4.0 is used. Timing capacitor C_T is chosen to be 1.0nF. For the desired converter frequency of 23kHz, Figure 6 indicates that a 45kΩ resistor should be used for R_C. The nearest standard value is 47kΩ. Dividing 47kΩ by the target R_C / R_D ratio of 4.0, R_D should then be 11.75kΩ. The nearest standard value is 12kΩ. Using 47kΩ and 12kΩ yields an R_C / R_D ratio of 3.92. Using 5% resistors, the ratio could be as low as 3.54, which corresponds to a duty cycle of 70%. Since this does not provide any headroom above the required 70% duty cycle, a 51kΩ resistor will be used for R_C, yielding a nominal R_C/R_D ratio of 4.25, and a worst case R_C / R_D ratio of 3.85 which corresponds to a maximum duty cycle of 72%. Double-checking frequency using a 51kΩ resistor still results in a nominal converter frequency of about 23kHz.

Feedback Components R_{FB} & Z_{FB}

For maximum regulation, R_{FB} should be slightly higher than twice R_C. Since R_C is 51kΩ, R_{FB} should be slightly greater than 102kΩ. The next highest standard value is 110kΩ. Using 5% resistors, the R_{FB} / R_C ratio could be as low as 1.95, which does not meet the requirement that R_{FB} / R_C be greater that 2 under all conditions. The next highest value for R_{FB} is then 120kΩ, giving an R_{FB} / R_C ratio of 2.35. Again using 5% resistors, the R_{FB} / R_C ratio could be as low as 2.13, which meets the 2/1 requirement. An R_{FB} of 120kΩ is selected

Using an R_C / R_D of 4.25 and an R_{FB} / R_C of 2.35, Figure 9 indicates that $V_{BIAS(max)}$ will be about 2.1 times the supply voltage. Zener voltage should then be V_{OUT} minus 1/2 $V_{BIAS(max)}$, or 147 - 152V over the input voltage range. The closest common Zener value is 150V and is used.

Figure 10: Example Circuit



** 330µH J.W. Miller PM105-331K*

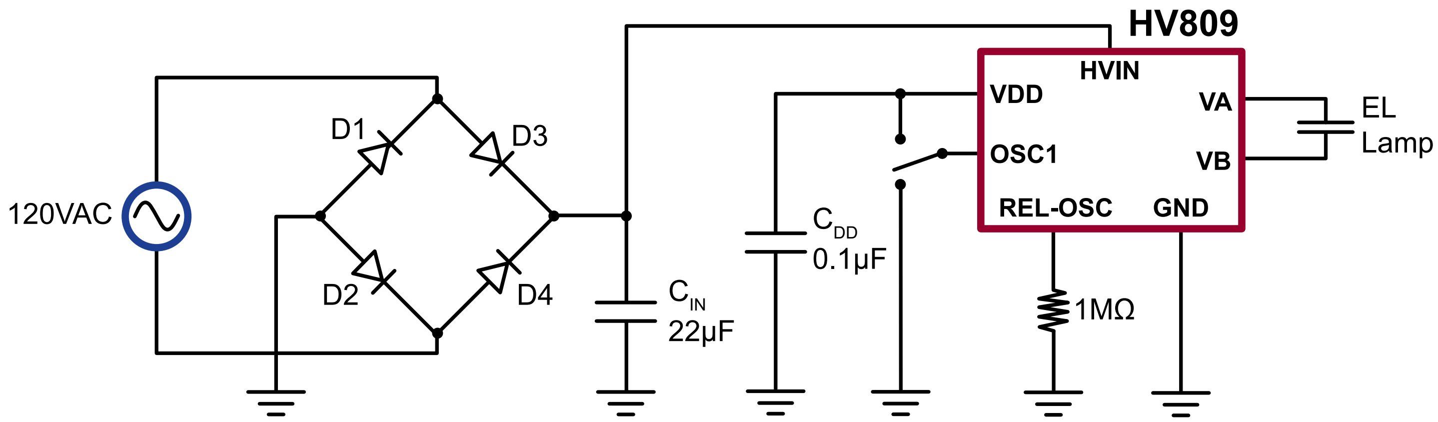
The Final Circuit

The final circuit using the selected components is shown above in Figure 10.

The circuit was built and tested with the following results:

Characteristic	Measured	Condition
Nominal output voltage	160.8V	V_{IN} = 5.25V, R_{LOAD} = 39.65kΩ
Line regulation	2.8%	V_{IN} = 4.5 - 6.0V, R_{LOAD} = 39.65kΩ
Load regulation	3.8%	V_{IN} = 5.25V, R_{LOAD} = 39.65kΩ - ∞
Efficiency	83%	V_{IN} = 5.25V, R_{LOAD} = 39.65kΩ
Nominal frequency	22.67kHz	V_{IN} = 5.25V, R_{LOAD} = 39.65kΩ
Frequency variation	±16%	V_{IN} = 4.5 - 6.0V, R_{LOAD} = 39.65kΩ
No-load frequency	2.769kHz	V_{IN} = 5.25V, R_{LOAD} = ∞

Figure 11: Off-line EL Lamp Driver



Section II - Off-line EL Lamp Driver

In this section, the Supertex HV809K2 is being used to drive a 100in^2 EL lamp from a rectified 120V AC line as shown in Figure 11. A brightness level of 20ft-L was measured. The HV809 is used to drive the EL lamp at 400Hz with a peak-to-peak voltage of 340V. In addition, the EL lamp can be turned on/off by logic level signals. Applications of this circuit can be for signage, courtesy lighting, and accent lighting.

General Circuit Description

The supply voltage is a 120VAC line which is full wave rectified to 170VDC. The 170VDC is used to power the HV809K2. The HV809K2 has an internal linear regulator to generate a V_{DD} supply which is at a nominal 10VDC. The V_{DD} supply is used to drive the internal low voltage CMOS oscillator circuit for the EL frequency. The EL frequency can be adjusted by an external resistor from $R_{EL\text{-}OSC}$ to ground. The CMOS oscillator controls the high voltage output h-bridge, V_A and V_B. The EL lamp is connected between V_A and V_B and is driven to a peak-to-peak voltage of ±170V at a frequency set by the external $R_{EL\text{-}OSC}$ resistor.

Calculations

The incoming 120V AC line is full wave rectified by diode bridge D1, D2, D3, and D4. The peak voltage for 120VAC line is 120V x 1.414 = 170V. The breakdown voltage for the diode bridge needs to be greater than 170V. 200V diodes or higher such as an industry standard 1N4003 are adequate.

C_{IN} is a 200V or higher electrolytic capacitor. Its capacitance value should be selected such that the ripple voltage is less than 20V to minimize heating of the capacitor. C_{IN} can be determined as follows:

$$C_{IN} = I_{IN} / (2 \cdot V_{RIPPLE} \cdot f_{LINE})$$

where: I_{IN} = *average current drawn from the* C_{IN} *capacitor*
V_{RIPPLE} = *maximum ripple voltage, 20V*
f_{LINE} = *line frequency, 60Hz*

The I_{IN} current is the HV809 operating current plus the load current. I_{IN} can be approximated with the following equations:

$$I_{IN} = I_{INQ} + (2 \cdot f_{EL} \cdot C_{EL} \cdot HV_{IN})$$

where: I_{INQ} = *operating current for the HV809*
f_{EL} = *EL lamp frequency*
C_{EL} = *EL lamp capacitance*
HV_{IN} = *input DC voltage*

The I_{INQ} for the HV809 is rated as 400μA maximum. An f_{EL} of 400Hz was selected because EL lamps are typically most efficient in the 400Hz range. Using a value of 3.5nF/in^2 of EL lamp material would be a good first order approximation for C_{EL}. For a 100in^2, C_{EL} would be 350nF. HV_{IN} has been calculated earlier as 170V.

$$I_{IN} = 400\mu A + (2 \cdot 400Hz \cdot 350nF \cdot 170V)$$
$$= 48mA$$

C_{IN} can now be estimated to be:

$$C_{IN} = 48mA / (2 \cdot 20V \cdot 60Hz)$$
$$= 20\mu F \text{ or larger}$$

C_{IN} was chosen to be 22μF, which is the closest standard value capacitor. The voltage waveform on C_{IN} is shown in Figure 12.

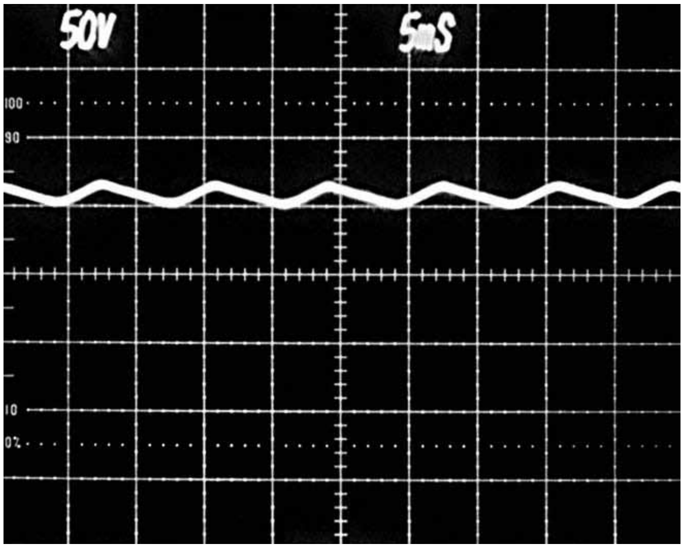


Figure 12: C_{IN} Voltage

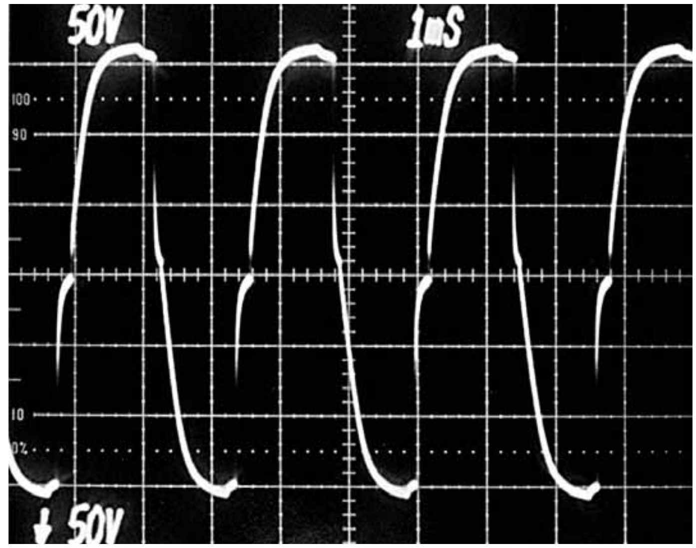


Figure 13: V_A - V_B Waveform

EL Lamp Frequency

An R_{EL} resistor value of 1.0MΩ will set the EL lamp frequency to a nominal value of 400Hz. The differential voltage waveform is shown in Figure 13. Increasing R_{EL} value will decrease the EL lamp frequency. EL lamp frequency range can be set from 100 to 1.2KHz. When adjusting for higher frequencies, it should be noted that the power dissipation will also increase.

OSC_1 Input

The output H-bridge can be enabled and disabled by connecting the OSC_1 pin to GND and VDD. The output can be left enabled by connecting OSC_1 to GND. The HV809 can be controlled by an external logic signal such as a microprocessor by using a low threshold MOSFET such as Supertex TN2106K1 with a 200KΩ pull-up resistor as shown in Figure 14.

Power Dissipation / Heat Sink Considerations

The input current, I_{IN}, was calculated to be 48mA at 170V DC. The input power is 170V times 48mA which is 8.16 Watts. The 8.16 Watts is distributed between the EL lamp and the HV809. The distribution depends on the parasitic series resistance of the EL lamp and the switch resistance of the HV809's H-bridge. Typically one third of the power is dissipated by the EL lamp and two thirds are dissipated by the HV809.

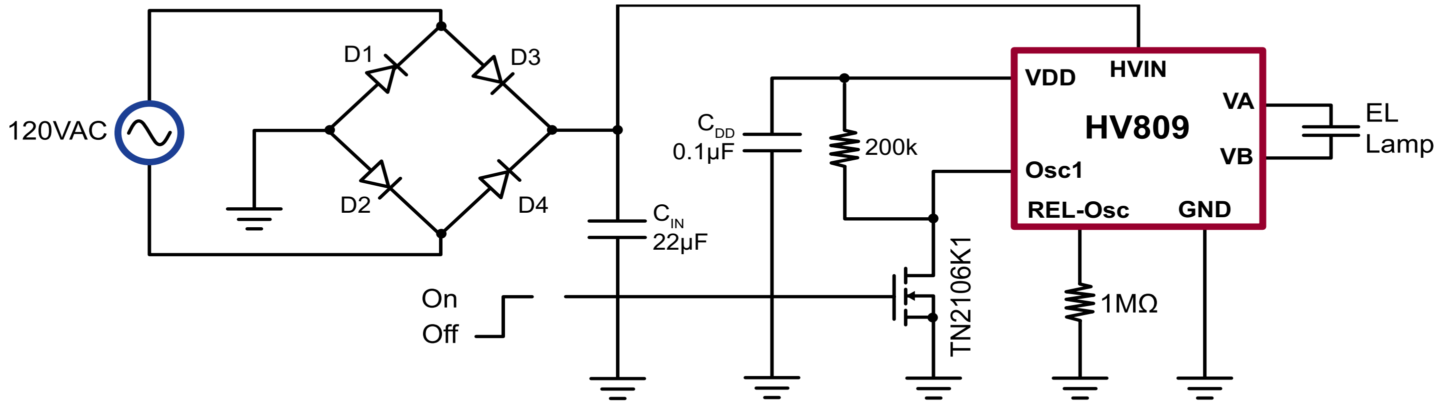
The HV809K2 is a 7-pin TO-220 package. With the appropriate heat sink, the maximum amount of power it can dissipate is 15 Watts at an ambient temperature of 25°C. Without any heat sinks (free air), the power dissipation is only 1.5 Watts at an ambient temperature of 25°C. The power dissipation limitation is set by the maximum allowable junction temperature of 150°C. The junction temperature can be calculated as follows:

$$T_J = P_{DISS} \times (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

where, T_J *= junction temperature*
P_{DISS} *= HV809 power dissipation*
θ_{JC} *= junction to case thermal resistance*
θ_{CS} *= case to heat sink thermal resistance*
θ_{SA} *= heat sink to air thermal resistance*
T_A *= Ambient temperature*

θ_{JC} is typically 5^{O}C/Watt, and is a function of the die size, the type of die attach material, and the leadframe material. θ_{CS} will depend on how the device is mounted on to the heat sink. Typically, silicone pads or thermal grease are used. θ_{SA} will depend on the size of the heat sink and any cooling methods such as forced air or liquid cooling.

Figure 14: Enable/Disable Implementation



For an ambient temperature of 25°C, a P_{DISS} of 15 Watts, and a maximum junction temperature of 150°C, the thermal resistance for case to heat sink plus heat sink to ambient needs to be less than 3.3°C/Watt. An 8.0in^3 vertical heat sink with natural convection would be sufficient.

There are many different stardard size heat sinks with various shapes available. It is advisable to request heat sink specifications from the manufacturers for help in selecting the most appropriate heat sink for a given specific application.

Conclusion

The ease of using the Supertex HV809 allows for quick circuit design. This application note has described how to design a simple DC-DC converter for battery-operated applications. The HV809 is a very powerful device capable of driving large EL lamps to high brightness. The HV809 in SO-8 package (HV809LG) is targeted to drive lamps used in hand held instruments when PCB area and height are important, and high brightness is required. The HV809 in the SO-8 package is limited by a maximum 500mW power dissipation when driving a large lamp to very high brightness. The HV809K2 in the 7-pin TO-220 package is suitable for larger, brighter lamps, as it can dissipate up to 15W with a heat sink.

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