Avoiding Turn-on Oscillations in the HV91 Family of PWM ICs

Introduction

Since there is no hysteresis in the undervoltage shutdown in the Supertex HV91 series of converters, there may be situations where insufficient power is provided to the V_{DD} terminal of the chip by the power supply on its first cycle to replace the charge that was removed from the V_{DD}-to-V_{SS} capacitor to drive the MOSFET on its first cycle. As a consequence of the lower VDD caused by driving the MOSFET, the undervoltage shutdown is triggered and the PWM shuts off, until the energy in the capacitor is replenished via the internal depletion-mode starting FET. This condition is more prevalent when the HV91 must drive a large MOSFET, and the V_{DD} capacitor is an electrolytic and located some distance from the IC, or is heavily loaded externally, as can be the case when the V_{DD} supply for the PWM is also used by a load the power supply is powering.

There are a couple of methods of preventing this turn-on oscillation. The simplest is to use a capacitor with very good high frequency performance and that is sized to slightly more than 100 times the effective gate capacitance (not the C_{ISS}) of the MOSFET being driven. Mount it very close to the V_{DD} and V_{SS} terminals. To determine the effective gate capacitance of the MOSFET, find the total gate charge on the "Gate Charge vs. Gate Voltage" graph on the MOSFET data sheet and, using the V_{DD} of the HV91 as a gate voltage divide gate charge by gate voltage to determine effective gate capacitance. (It will be a larger value than C_{ISS}.) A good stacked film capacitor of 100 times the effective gate capacitance should prevent the oscillations.

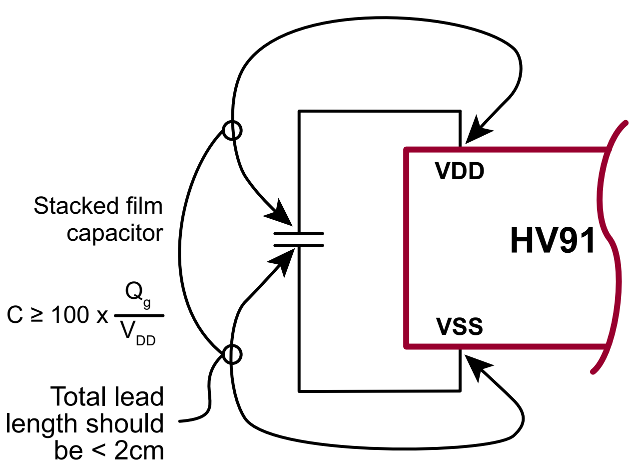

Figure 1: The Easy Way

If the previous solution is not possible, there is a second solution that is almost as simple, but it requires a bit more calculation.

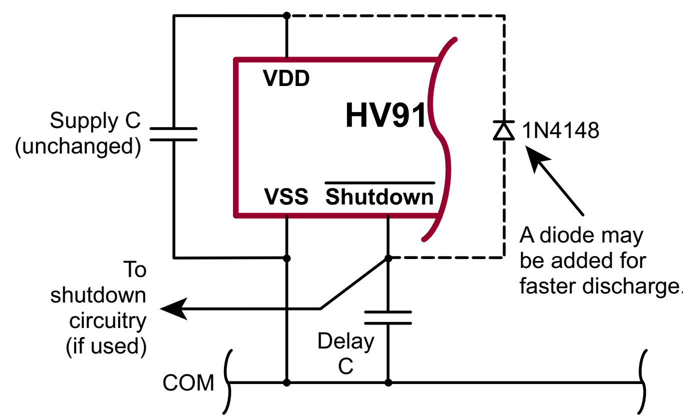

Figure 2: A Turn-On Delay

The shutdown terminal of the HV91 has an internal current source that is normally used only to keep the pin high so that it can be ignored when remote shutdown is not used. This current source will source approximately 50% of the current being drawn from the bias pin by the bias setting resistor (see Figure 3 on the data sheet to determine IC bias current). Placing a delay capacitor on the shutdown terminal will delay the normal turn-on of the HV91 until V_{DD} has risen high enough so that the capacitor on the V_{DD} line can supply the power necessary to drive the MOSFET without V_{DD} falling so low that the undervoltage turns the PWM off again.

To determine the size of capacitor required, first calculate how long it will take for V_{DD} to rise to where it will not be turned off by a slight droop. Generally this time (in seconds) will be 500 to 1000 times the value of the capacitor (in farads) connected between the VDD and VSS pins. The value of the delay capacitor then can be calculated from:

$$C_{DELAY} = \frac{t_{DELAY} \cdot I_{BIAS}}{V_{DD}}$$

To discharge the delay capacitor, many schemes can be used. Two of the simplest are to use a diode from shutdown to V_{DD} (though this can be disrupted by very short drops in power) or to use an active discharge.

If rapid power cycling is expected, an active discharge such as that shown in Figure 3 can be used. This circuit uses a 2N6027 programmable unijunction transistor, which, when V_{DD} drops approximately 0.7V below the voltage on the delay capacitor, quickly discharges the delay capacitor.

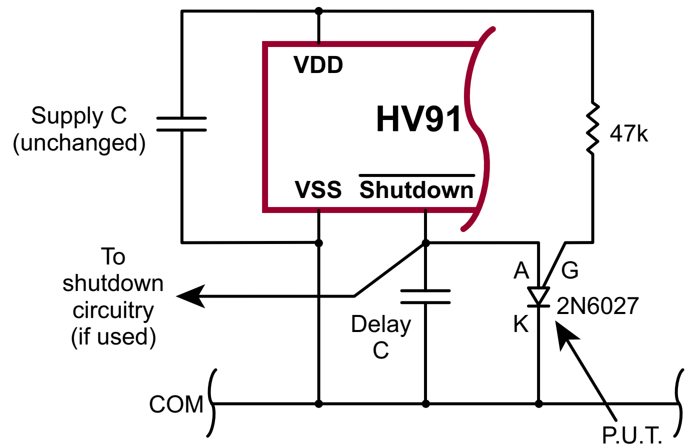

Figure 3: Active Discharge

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