Calculating Power Dissipation and Supply Current in HV91 Series Parts

Part I

The internal circuitry of the HV9110/11/12/13 and HV9120/23 uses very little current by itself - generally less than 1.0mA. However, when driving a large MOSFET very fast, considerable current can be demanded from the V_{DD} supply for the chip. The total current required is the sum of three component currents: the first two component currents, quiescent supply current and clock current, generally total less than 1.0mA, while the third, the MOSFET drive current, can vary considerably and is generally responsible for most of the current required for operation of the chip. Reasonably accurate values for the current consumed by the internal circuitry and the clock oscillator can be taken from the graphs of quiescent I_{DD} vs. R_{BIAS} current (Figure 1) and oscillator current vs. R_{OSC} (Figure 2). The MOSFET drive current must be calculated.

Calculating the current needed to drive the MOSFET is straight forward, but requires using the “Total Gate Charge vs. Gate-Source Voltage” graph from the MOSFET’s data sheet. The calculation proceeds as follows:

First, the operational V_{DD} the IC will use should be known. This is generally a parameter decided upon by the designer for his convenience. Once V_{DD} is known, it is used to find the total gate charge of the MOSFET by using V_{DD} for the gate voltage. Dividing total charge by gate voltage calculates the effective gate capacitance of the MOSFET at that gate voltage. (Because the output of the HV91 family PWMs swings rail-to-rail, V_{GATE} will be nearly equal to V_{DD}.

$$Q_{GATE} / V_{DD} = C_{GATE(effective)}$$

Next, a calculation of power can be made with the effective gate capacitance from the formula:

$$P_{DRIVE} = C_{GATE(effective)} \bullet V_{GATE}^{2} \bullet f$$

where f is the operating frequency of the converter. Adding the power calculated in this step to the two other components of total power (for clock and quiescent power this is merely the current found on the graph, multiplied by V_{DD}) gives the

Figure 1

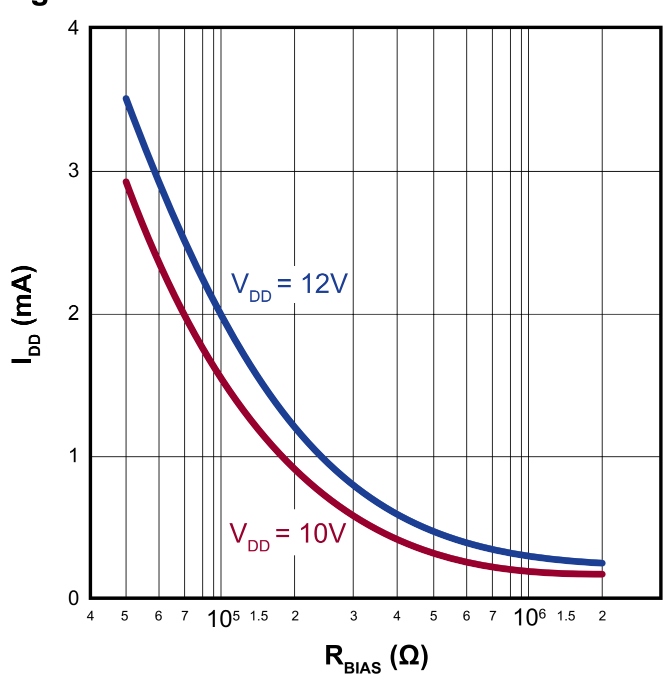
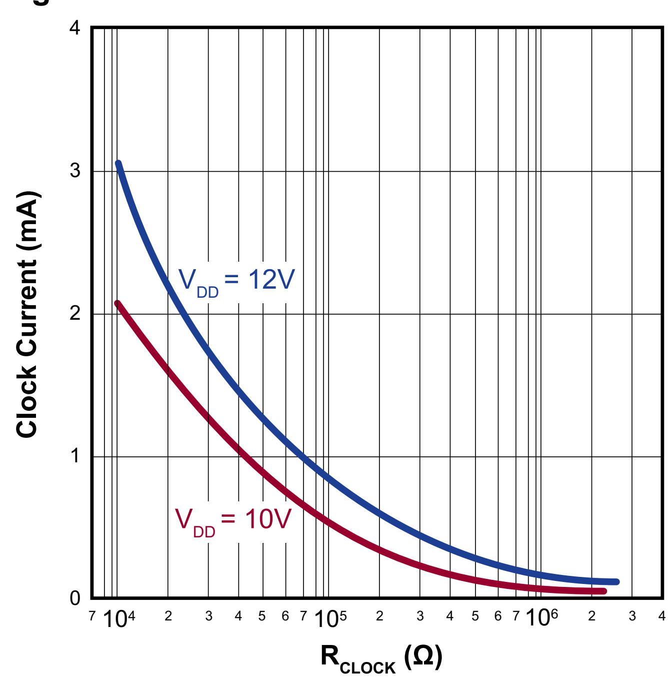


Figure 2



total power dissipated in the IC:

$$P_{TOTAL} = P_{QUIESCENT} + P_{CLOCK} + P_{DRIVE}$$

$$P_{QUIESCENT} = I_{DD(quiescent)} \cdot V_{DD}$$

$$P_{CLOCK} = I_{DD(clock)} \cdot V_{DD}$$

$$P_{DRIVE} = C_{GATE(effective)} \cdot V_{DD2} \cdot f$$

Drive power is actually dissipated almost entirely in the IC, and not in the gate of the MOSFET, because what dissipates the power in an R-C circuit is the resistance, not the capacitance. The gate resistance of a MOSFET is quite low (usually less than 0.05Ω) when compared to the on resistance of the driver that is driving it (typically 15 to 20Ω for the HV91 family) so calculations which neglect MOSFET gate resistance will generally be off by less than 1%. The reason the 1/2 is missing from the familiar $E = 1/2\ CV^2$ equation is that the driver dissipates power both in charging and discharging the MOSFET gate. If a series resistor is used between the gate of the MOSFET and the PWM IC, then the dissipation is divided between the PWM IC and the gate resistor in proportion to their resistance. Gate resistors are not ecommended, however, when a MOSFET is being driven from CMOS drivers like the HV91 family devices. A gate resistor will only slow down the rate of rise and fall of gate voltage, which will increase switching losses in the MOSFET and reduce system efficiency.

To calculate the current load on the power supply that supplies power to the IC, divide the total power dissipated in the IC by V_{DD} to produce a current required from the supply. The drive portion of the current will be taken in pulses, with peaks many times the DC rate, but the DC current can be used to calculate the load on the supply because the capacitor between V_{DD} and V_{SS} of the IC serves as a reservoir for the energy required. This also shows why that capacitor must have excellent high frequency performance. Incidentally, this procedure can be used to define a reasonable minimum size for the V_{DD} to V_{SS} capacitor: 100 x $C_{GATE(effective)}$ is a good minimum value. Usually, for reasons having to do with regulator loop stability or output ripple, a larger capacitor will be required. This formula defines the smallest capacitor that is practical to use.

Examples

Example 1: An HV9120 using a 1.2MΩ bias resistor, a V_{DD} of 10V, and driving a Supertex VN2460 MOSFET at 20kHz. From Figure 1, with a bias resistor of 1.2MΩ, quiescent I_{DD} will be 275µA. The data sheet curve for R_{CLOCK} vs. frequency shows that 820kΩ is an appropriate clock resistor value for operation at 20kHz. Figure 2 shows that this will require an additional 160µA of I_{DD}.

From the VN2460 data sheet, Q_G will be 5.5nC at maximum drain voltage. Dividing by the 10V V_{DD} gives an effective gate capacitance of 550pF. Now the three components of power can simply be calculated as follows:

$$P_{DRIVE} = 550 \times 10^{-12}F \cdot 10V^2 \cdot 20{,}000Hz = 1.10mW$$

$$P_{QUIESCENT} = 275\mu A \cdot 10V = 2.75mW$$

$$P_{CLOCK} = 160\mu A \cdot 10V = 1.6mW$$

Summing the three dissipations gives a total chip power dissipation of 5.45mW. Dividing by 10V gives a total I_{DD} requirement of 545µA. That is all the power needed to operate under this simple set of conditions.

Example 2: An HV9113 using a bias resistor of 100kΩ and a V_{DD} of 12V, driving an IRF630 at 750KHz.

Again from Figure 1, a bias resistor of 100kΩ with a 12V V_{DD} requires a quiescent I_{DD} of 2.0mA. This time, the appropriate clock resistor (from the data sheet graph) will be 36kΩ, and, from Figure 2, this will require an additional I_{DD} of 1.6mA.

From the data sheet for the IRF630, total gate charge (Q_G) with V_{GATE} = 12V will be 22nC at maximum drain voltage. Dividing by 12V gives an effective gate capacitance of 1.83nF, and the power dissipation will be:

$$P_{DRIVE} = 1.83 \cdot 10\text{-}9F \cdot 12V2 \cdot 750{,}000Hz = 0.198W$$

$$P_{QUIESCENT} = 0.002A \cdot 12V = 0.024W$$

$$P_{CLOCK} = 0.0016A \cdot 12V = 0.0192W$$

Summing gives a total dissipation of 241.2mW, and dividing by V_{DD} gives a total I_{DD} requirement of 20.1mA. This set of operating conditions is more demanding than those of the first example, but is still well within the dissipation limits of the part. It also serves to demonstrate that, when using very large MOSFETs in a very high frequency power supply, it is better to use a separate driver IC. It should also be noted that if C_{ISS} had been used for these calculations, instead of $Q_G \div V_{DD}$, the resulting total power calculation would have been less than half of the true power loss in the part.

Part II

The foregoing gives complete power dissipation for an HV91 family PWM IC when it is powered from its VDD terminal. Generally, this is how HV91 family parts are intended to be used, with power from VIN terminal used only for starting or for powering the PWM IC while it is in shutdown mode. (The VIN terminal actually shuts off when power is supplied to the VDD terminal.) In some cases, the HV91 family parts can be operated with power supplied to their VIN terminal. In such cases, extreme care must be taken not to overstress the part, as the maximum allowable voltage (on an HV9120, for instance) can be up to 450V, and the voltage drop between VIN and VSS results in power dissipation.

If you intend to operate an HV91 family part from its VIN terminal, first calculate the low-voltage current requirement according to the first part of this note; then, when the required input current is known, multiply that current by the maximum input voltage to calculate complete power dissipation.

$$I_{DD} \cdot V_{IN(max)} = P_{(max)}$$

For the first example, if we assume a maximum input voltage of 407V, then maximum dissipation will be:

$$0.000478A \cdot 407V = 0.195W$$

which is still reasonable for the part, but may not be reasonable from an efficiency standpoint, as it represents an increase of 40 times in power dissipation. In the second example, even with the constraint of the HV9113 only being capable of 120V max on its VIN terminal, the situation is very different:

$$0.0201A \cdot 120V = 2.412W$$

In this case, the HV9113 would burn up due to the excessive power.

As a general rule, because the V_{IN} regulator represents less than 1/4 of the total chip area of the IC, it is not practical for it to provide more than 25% of total package power dissipation on a continuous basis. For the plastic DIP, this works out to 250mW continuously. So, actually, the second example is worse than it looks. If we assume that the 20.1mA remains constant (in practice, it will go down somewhat, as the original power calculations were based on a V_{DD} of 12V, and when running an HV91 series PWM from the VIN terminal, V_{DD} will be approximately 9.2V) the maximum input voltage that will hold continuous dissipation in the input regulator to 250mW is 21.6V. This may still be useful in some circumstances, but illustrates how quickly power dissipation in the input regulator can get out of hand. It is much better, when operating an HV91 family part, to have power for continuous operation supplied to the VDD terminal from the supply it is controlling. Either mode of operation is possible, but using the V_{DD} is more efficient, and there are no problems even at high frequencies or with large loads.

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