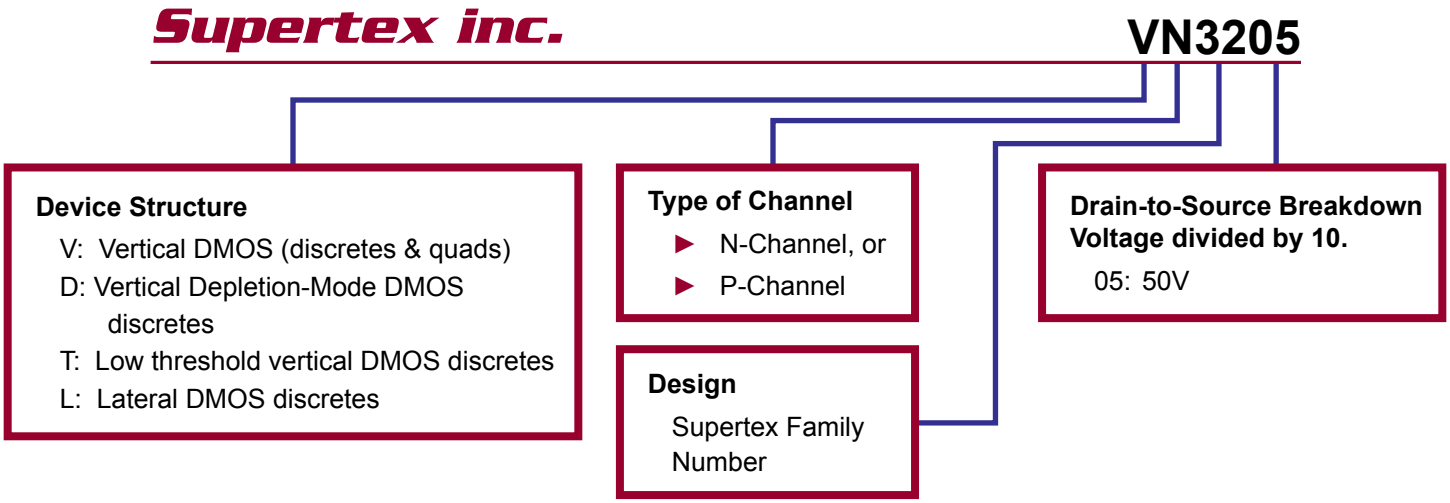
Understanding MOSFET Data

The following outline explains how to read and use Supertex MOSFET data sheets. The approach is simple and care has been taken to avoid getting lost in a maze of technical jargon.

The VN3205 data sheet was chosen as an example because it has the largest choice of packages. The product nomenclature shown applies only to Supertex proprietary products.



Advanced DMOS Technology

This enhancement-mode (normally-off) DMOS FET transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speed are desired.

This section outlines main features of the product.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Device	Package Options				BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ max (Ω)	$I_{D(ON)}$ min (A)
	TO-92	14-Lead PDIP	TO-243AA (SOT-89)	Die			
VN3205	VN3205N3-G	VN3205P-G	VN3205N8-G	VN3205ND	50	0.3	3.0

Drain to source breakdown voltage & drain to gate breakdown voltage.

Maximum resistance from drain to source when device is fully turned on.

Minimum drain current when device is fully turned on.

Package Options

TO-92

- Low power
- Plastic
- Cost effective
- Mainly commercial applications

SOT-89

- Low profile
- Low θ_{JC} thermal resistance
- Commercial and industrial applications

Ordering Information

Device	Package Options				BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ max (Ω)	$I_{D(ON)}$ min (A)
	TO-92	14-Lead PDIP	TO-243AA (SOT-89)	Die			
VN3205	VN3205N3-G	VN3205P-G	VN3205N8-G	VN3205ND	50	0.3	3.0

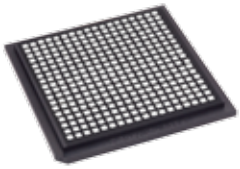
14-Lead DIP

- Dual in line plastic
- 4 die in one package
- Commercial and industrial applications

Wafer

- NW: Die in wafer form
- 6 inch diameter wafers
- Reject dice are inked

Waffle Pack



- ND: die in waffle pack
- Die can be visually inspected to commercial (standard) or military visual criteria (specify while ordering)

Absolute Maximum Ratings

Extreme conditions a device can be subjected to electrically and thermally. Stress in excess of these ratings will usually cause permanent damage.

Ratings given in product summary.

V_{GS}

- Most Supertex FETs are rated for ±20V.
- ±voltage handling capability allows quick turn off by reversing bias.
- External protection should be used when there is a possibility of exceeding this rating. Stress exceeding ±20V will result in gate insulation degradation and eventual failure.

- All Supertex devices can be stored and operated satisfactorily within these junction temperature (T_J) limits.
- Appropriate derating factors from curves and change in parameters due to reduced/elevated temperatures have to be considered when temperature is not 25°C.
- Operation at T_J below maximum limit can enhance operating life.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *Distance of 1.6mm from case for 10 seconds.*

Maximum allowable temperature at leads while soldering, 1.6mm away from case for 10 seconds.

Thermal Characteristics

Device characteristics affecting limits of heat produced and removed from device. Die size, $R_{DS(ON)}$ and packaging type are the main factors determining these thermal limitations.

Thermal Characteristics

Package	I_D (continuous)* (A)	I_D (pulsed) (A)	Power Dissipation @T_C = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (A)	I_{DRM} (A)
TO-92	1.2	8.0	1.0	125	170	1.2	8.0
14-Lead PDIP	1.5	8.0	3.0†	41.6†	83.3†	1.5	8.0
TO-243AA	1.5	8.0	1.6 (T_A = 25°)	15	78‡	1.5	8.0

Notes:

* I_D (continuous) is limited by max rated T_J, T_A = 25°C.

† Total for package.

‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm.

I_D (continuous)

Maximum continuous current carrying capability of device.

Depends mainly on:

- $R_{DS(ON)}$ - on state resistance.
- P_D - maximum power dissipation for package.
- Die size.
- Maximum junction temperature.

ID (pulsed)

Maximum non-continuous pulse current carrying capability for a 300µs 2% duty cycle pulsed.

Depends mainly on:

- $R_{DS(ON)}$.
- P_D max.
- Diameter of bonding wire.
- Die size.
- Maximum junction temperature.

Power Dissipation

- Maximum power package can dissipate when case temperature is 25°C.
- When case temperature is higher than 25°C, use P_D vs. T_C curve to determine dissipation permissible.

I_{DRM}

300µs, 2% duty cycle pulsed. Current handling capability of drain source diode.

- Factors affecting value same as I_D (pulsed).

I_{DR}

Continuous current handling capability of drain to source diode.

- Factors affecting value same as I_D (continuous).

θ_{JA}

Thermal resistance from junction to air.

- Depends mainly on package and die size.

θ_{JC}

Thermal resistance from junction to case.

- Depends mainly on package and die size
- To determine T_J use equation:

$$T_J = P_D \times \theta_{JC} + T_C$$

Electrical Characteristics

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage		50	-	-	V	V_{GS} = 0V, I_D = 10mA
$V_{GS(th)}$	Gate threshold voltage		0.8	-	2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature		-	-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate body leakage current		-	1.0	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current		-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
			-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current		3.0	14	-	A	V_{GS} = 10V, V_{DS} = 5.0V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	TO-92 and PDIP	-	-	0.45	Ω	V_{GS} = 4.5V, I_D = 1.5A
		TO-243AA	-	-	0.45		V_{GS} = 4.5V, I_D = 0.75A
		TO-92 and PDIP	-	-	0.3		V_{GS} = 10V, I_D = 3.0A
		TO-243AA	-	-	0.3		V_{GS} = 10V, I_D = 1.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature		-	0.85	1.2	%/°C	V_{GS} = 10V, I_D = 3.0A
G_{FS}	Forward transconductance		1.0	1.5	-	mho	V_{DS} = 25V, I_D = 2.0A
C_{ISS}	Input capacitance		-	220	300	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance		-	70	120		
C_{RSS}	Reverse transfer capacitance		-	20	30		
$t_{d(ON)}$	Turn-on delay time		-	-	10	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 10Ω
t_r	Rise time		-	-	15		
$t_{d(OFF)}$	Turn-off delay time		-	-	25		
t_f	Fall time		-	-	25		
V_{SD}	Diode forward voltage drop		-	-	1.6	V	V_{GS} = 0V, I_{SD} = 1.5A
t_{rr}	Reverse recovery time		-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

BV_{DSS}

- Please see product summary (part I).
- Positive temperature coefficient. See curve BV_{DSS} vs. T_J.

$V_{GS(TH)}$

- Voltage required from gate to source to turn on device to certain I_D current value given in “condition” column.
- I_D measurement condition is low for small die and higher for larger die.

I_{GSS}

- Since the gate is insulated from the rest of device by a silicon dioxide insulating layer, this parameter depends on thick-ness/integ rity of layer and size of device.
- Measured at maximum permissible voltage from gate to source: ±20V.
- Values of this parameter are often tens/hun-dreds of times less than pub lished maxi-mum value. Electrical screening is done at 100nA since test equipment functions slowly at lower values, which is not practical for mass production. Consult factory for screen-ing lower values.

$\Delta V_{GS(TH)}$

- Threshold voltage reduces when tempera-ture increases and vice versa.
- Value at temperature other than 25°C can be determined by $V_{GS(TH)}$ (normalized) vs. T_J curve.

Electrical Characteristics

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage		50	-	-	V	V_{GS} = 0V, I_D = 10mA
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I_{DSS}	Zero gate voltage drain current		-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
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$I_{D(ON)}$	On-state drain current		3.0	14	-	A	V_{GS} = 10V, V_{DS} = 5.0V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	TO-92 and PDIP	-	-	0.45	Ω	V_{GS} = 4.5V, I_D = 1.5A
		TO-243AA	-	-	0.45		V_{GS} = 4.5V, I_D = 0.75A
		TO-92 and PDIP	-	-	0.3		V_{GS} = 10V, I_D = 3.0A
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$t_{d(ON)}$	Turn-on delay time		-	-	10	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 10Ω
t_r	Rise time		-	-	15		
$t_{d(OFF)}$	Turn-off delay time		-	-	25		
t_f	Fall time		-	-	25		
V_{SD}	Diode forward voltage drop		-	-	1.6	V	V_{GS} = 0V, I_{SD} = 1.5A
t_{rr}	Reverse recovery time		-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

I_{DSS}

- This is the leakage current from drain to source when device is fully turned off.
- Measured by applying maximum permissible voltage between drain and source (BV_{DSS}) and gate shorted to source (V_{GS} = 0).
- Special electrical screening possible at lower values since max. published values are higher to achieve practical testing speeds.

$I_{D(ON)}$

- Defined as the minimum drain current when device is turned on.
- Supertex measures $I_{D(ON)}$ min. at V_{GS} = 10V.

  Although Supertex specifies a typical value of $I_{D(ON)}$, the designer should use minimum value as the worst case.

$\Delta R_{DS(ON)}$

- Positive temperature coefficient.
- Enhances stability due to current sharing during parallel operation.

$R_{DS(ON)}$

- Drain to source resistance measured when device is partially turned on at V_{GS} = 4.5V, and fully turned on at V_{GS} = 10V.
- Designers should use maximum values for worst case condition.
- When better turn on characteristics (ie., low $R_{DS(ON)}$) is required for logic level inputs, Supertex's low threshold TN & TP devices may be used.
- Typical value of $R_{DS(ON)}$ can be calculated at various V_{GS} conditions by using output characteristics or saturation characteristics family of curves (I_D vs. V_{DS}).
- $R_{DS(ON)}$ increases with higher drain currents. $R_{DS(ON)}$ curve has a slight slope for low values of I_D, but rises rapidly for high values.

Switching Characteristics

- Extremely fast switching compared to bipolar transistors, due to absence of minority carrier storage time during turn off.
- Switching times depend almost totally on interelectrode capacitance, R_S (source impedance) and R_L (load impedance) as shown on test circuit.

G_{FS}

- Represents gain of the device and can be compared to H_{FE} of a bipolar transistor.
- Value is the ratio of change in I_D for a change in V_{GS}:

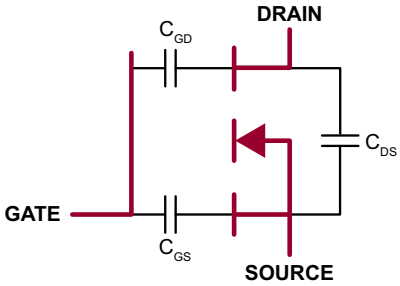
$$G_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- Rises rapidly with increasing I_D, and then becomes constant in the satur-ation region. See G_{FS} vs. I_D curve.

C_{ISS}, C_{RSS}, C_{OSS}

- Supertex interdigitated structures have lowest C_{ISS} in the industry for comparable die sizes and exhibit excellent switching characteristics.
- Values of these capacitances are high at low voltages across them. Please see capacitance vs V_{DS} curves for details.
- Negligible effect of temperature on capacitances.
- The following equation may be used for calculating effective value of C_{ISS} with "Miller Effect."

$$C_{ISS} = C_{GS} + (1+G_{FS} \cdot R_L)\, C_{GD}$$



$$C_{ISS} = C_{GD} + C_{GS}$$
$$C_{OSS} = C_{GD} + C_{DS}$$
$$C_{RSS} = C_{GD}$$

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter		Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage		50	-	-	V	V_{GS} = 0V, I_D = 10mA
$V_{GS(th)}$	Gate threshold voltage		0.8	-	2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature		-	-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate body leakage current		-	1.0	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current		-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
			-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current		3.0	14	-	A	V_{GS} = 10V, V_{DS} = 5.0V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	TO-92 and PDIP	-	-	0.45	Ω	V_{GS} = 4.5V, I_D = 1.5A
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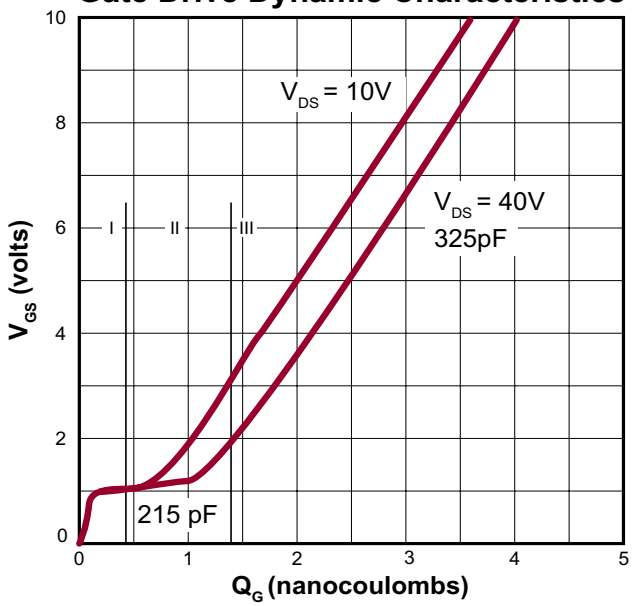
C_{ISS}	Input capacitance		-	220	300	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance		-	70	120		
C_{RSS}	Reverse transfer capacitance		-	20	30		
$t_{d(ON)}$	Turn-on delay time		-	-	10	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 10Ω
t_r	Rise time		-	-	15		
$t_{d(OFF)}$	Turn-off delay time		-	-	25		
t_f	Fall time		-	-	25		
V_{SD}	Diode forward voltage drop		-	-	1.6	V	V_{GS} = 0V, I_{SD} = 1.5A
t_{rr}	Reverse recovery time		-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

$T_{d(ON)}$

During this period, the drive circuit charges C_{ISS} up to $V_{GS(TH)}$. Since no drain current flows prior to turn on, V_{DS} and consequently C_{ISS} remain constant. Region I on the V_{GS} vs. Q_G curve shows linear change in voltage with increasing Q_G.

Gate Drive Dynamic Characteristics



Switching Characteristics

t_r

- When C_{ISS} is driven to a voltage exceeding $V_{GS(TH)}$, conduction from drain source begins. G_{FS} increases causing increase in C_{ISS} due to "Miller Effect" charge requirements to Region II increase considerably. Gain stabilizes in Region III and "Miller Effect" is nullified, resulting in a linear change in V_{GS} for increase in Q_G.

$t_{d(OFF)}$

- The sequence of events now begins to reverse. C_{ISS} discharges through R_{GEN}. The rise of V_{DS} is initially slowed by increase of output capacitance.

t_f

- V_{DS} rises as the load resistor charges the output capacitance.

V_{SD}

- This is the forward voltage drop of the parasitic diode between drain and source.
- Diode may be used as a commutator in H bridge configurations or in a synchronous rectifier mode. Excessive fly back voltages may be clamped by this diode in a totem pole configuration.

t_{rr}

- The reverse recovery time is the time needed for the carrier gradient, formed during forward biasing, to be depleted when the biasing is reversed.
- An external fast recovery diode may be connected from drain to source to improve recovery time.

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage		50	-	-	V	V_{GS} = 0V, I_D = 10mA
$V_{GS(th)}$	Gate threshold voltage		0.8	-	2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature		-	-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
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I_{DSS}	Zero gate voltage drain current		-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
			-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current		3.0	14	-	A	V_{GS} = 10V, V_{DS} = 5.0V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	TO-92 and PDIP	-	-	0.45	Ω	V_{GS} = 4.5V, I_D = 1.5A
		TO-243AA	-	-	0.45		V_{GS} = 4.5V, I_D = 0.75A
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$t_{d(ON)}$	Turn-on delay time		-	-	10	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 10Ω
t_r	Rise time		-	-	15		
$t_{d(OFF)}$	Turn-off delay time		-	-	25		
t_f	Fall time		-	-	25		
V_{SD}	Diode forward voltage drop		-	-	1.6	V	V_{GS} = 0V, I_{SD} = 1.5A
t_{rr}	Reverse recovery time		-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

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