Application Note

Low Dropout 3.0 Volt Linear Regulator

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Introduction

Low dropout regulators are becoming increasingly important as more and more equipment utilizes 3.0 and 5.0V analog and digital circuits.

The main advantage of low dropout 3.0V linear regulators is full utilization of battery life which makes them desirable for battery-powered applications. The low dropout feature will allow for output regulation even when the input battery voltage is discharged close to its output regulated voltage. This will extend the operating input voltage range and allow circuits to operate at a lower battery voltage.

This application note discusses the advantages of using Supertex part number LP0701N3, which is a very low gate threshold voltage P-Channel MOSFET. This part has a guaranteed maximum threshold of -1.0V and a maximum $R_{DS(ON)}$ of 2.0Ω at -3.0V drive. This performance is essential for designing an ultralow dropout, low voltage linear regulator.

Circuit Description

The low dropout 3.0V linear regulator shown on Figure 1 utilizes an LP07, an LM10, 4 resistors, and 3 capacitors. The LP07 is a 16.5V, 2.0Ω, P-Channel MOSFET with a maximum threshold of -1.0V. The LM10 is a dual op-amp with a 0.2V reference. R_1 is a potentiometer. R_2, R_3, and R_4 are 5%, 1/4 watt resistors. C_1, C_2, and C_3 can be either ceramic or electrolytic capacitors.

A_1 is configured as a unity gain buffer for the 0.2V reference. The output of A_1 is attenuated by R_1 and R_2 and is connected to the inverting input of A_2. A_2 is configured as a noninverting amplifier with a closed-loop gain of $(R_4/R_3 + 1)$. The LP07 is configured as a common source amplifier, which functions as a series pass transistor while contributing additional gain to the open-loop gain of A_2. The output of A_2 regulates the gate of LP07 for a V_{OUT} of $0.2V \times [R_1/(R_1 + R_2) \times (R_4/R_3 + 1)]$. The resistor values are chosen (explained in detail in the design considerations section of this application note) and R_1 adjusted for an output voltage of 3.0V. C_3 is in parallel with R_4 to reject external noise. C_1 and C_2 are bypass capacitors.

Any small decrease in V_{OUT} due to a load applied to the output is sensed by R_3 and R_4 which is fed back to the noninverting input of A_2. The output of A_2 will drive the gate of the LP07 to a lower potential thereby increasing the gate drive adequately to source current to the output load and maintain a constant output voltage.

Design Considerations

The objective is to implement a 3.0V linear regulator with the lowest possible voltage drop from input to output. The output transistor for a linear regulator can be designed with N-Channel or P-Channel MOSFETs or bipolar NPN or PNP transistors. Figures 2A to 2D show the four possibilities.

In Figure 2A, the dropout voltage using an N-Channel MOSFET is too large since it cannot be better than the threshold voltage of the MOSFET, which is 1.0 to 4.0V, depending on the type of device used. In figure 2b, the dropout voltage using an NPN is lower but still fairly large. The dropout voltage is typically 0.7V, which is the V_{BE} rating of the transistor.

In Figure 2C, the dropout voltage using a PNP transistor is limited by the $V_{CE(sat)}$ rating of the transistor, which is typically -200mV at low collector current. This approach also requires the output of the op-amp to operate 0.7V below its most positive rail at all times.

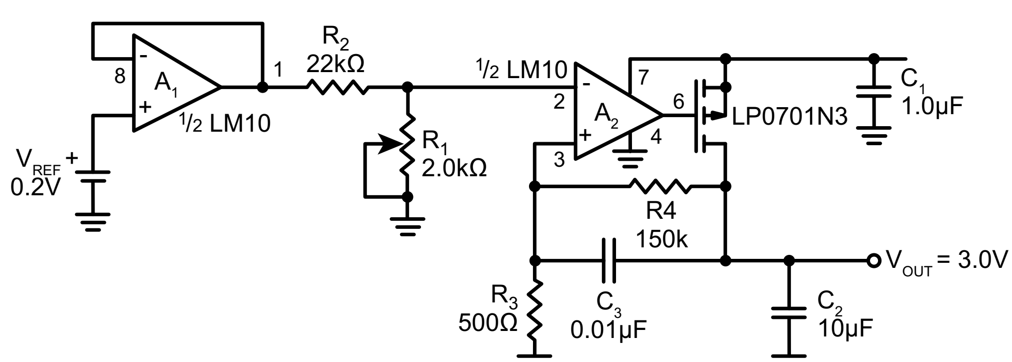


Figure 1: Low Dropout 3.0V Linear Regulator

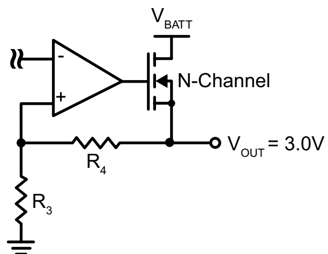


Fig 2A:
N-Channel MOSFET

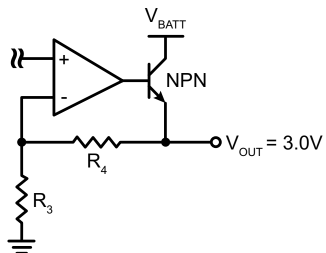


Figure 2B:
NPN Transistor

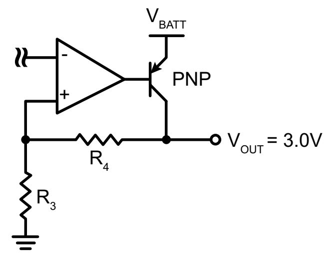


Figure 2C:
PNP Transistor

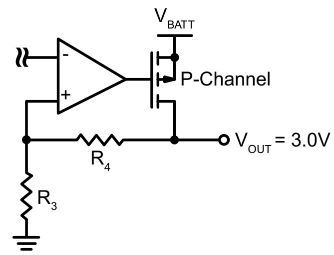


Fig 2D:
P-Channel MOSFET

In Figure 2D, the dropout voltage for the P-Channel MOSFET approach is determined by the on-resistance of the device times the load current. The device is driven by the battery voltage minus the minimum output voltage of the op-amp. Similar to the PNP approach, the op-amp is required to operate one threshold below the battery voltage during the no load condition. When the battery voltage is discharged close to 3.0V, the MOSFET chosen should have a very low threshold and a very low on-resistance at low V_{GS} ratings to achieve low dropout.

Conventional P-Channel MOSFETs have guaranteed maximum thresholds of -4.0V, which would require the supply voltage to be greater than 4.0V for adequate turn on. A low threshold, low on-resistance P-Channel MOSFET is ideal for this approach.

The Supertex LP07 has a guaranteed maximum threshold of -1.0V and guaranteed on-resistance at -2.0V, -3.0V, and -5.0V drives. The specifications are shown on the following table:

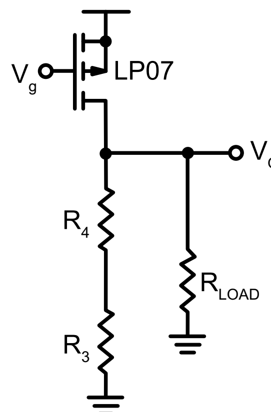
Parameter	Min	Typ	Max	Units	Conditions
$V_{GS(th)}$	-0.5	-0.7	-0.1	V	$V_{GS} = V_{DS}$, I_D = -1.0mA
$R_{DS(ON)}$	-	2.0	4.0	Ω	V_{GS} = -2.0V, I_D = -50mA
	-	1.7	2.0	Ω	V_{GS} = -3.0V, I_D = -150mA
	-	1.3	1.5	Ω	V_{GS} = -5.0V, I_D = -300mA

At -3.0V, the on-resistance is 1.7Ω typical and 2.0Ω maximum, which helps achieve a low drain-to-source voltage drop. Since the LM10 can swing very close to ground i.e., 0V, the dropout voltage can be estimated to be 2.0Ω x (I_{LOAD}). For a 50mA load, the dropout voltage is 0.1V which means the battery voltage can be 3.1V with the output still regulated at 3.0V.

Preventing Unwanted Oscillation

The LP07 acts as an additional gain stage to the open-loop gain of A_2. The increase in open-loop gain causes the loop gain to be greater than 1 at low closed-loop gain conditions, which causes oscillation. Oscillation can be eliminated by setting the loop-gain to be less than 1. This can be achieved by setting ß(negative feedback) < 1 / gain contributed by the LP07.

The gain contributed by the LP07 is a function of the load and the transconductance, G_{FS}, of the LP07. Figure 3 shows an equivalent circuit of the open-loop gain of the LP07.



$$G_{FS} = \frac{\delta I_d}{\delta V_g}$$

$$V_{OUT} = I_d \left[\frac{(R_3 + R_4)(R_{LOAD})}{R_3 + R_4 + R_{LOAD}} \right]$$

$$\frac{V_{OUT}}{V_g} = G_{FS} \left[\frac{(R_3 + R_4)(R_{LOAD})}{R_3 + R_4 + R_{LOAD}} \right]$$

Figure 3: LP07 Open-Loop

The G_{FS} of the LP07 varies with I_D, which is also the load current. Typical G_{FS} versus I_D for low and high currents of the LP07 is shown on figure 4a and 4b respectively.

For the no load condition, $I_D = 3.0V/(R_3 + R_4)$. It is desirable have $R_3 + R_4$ large to minimize the amount of biasing current. The sum of $R_3 + R_4$ is chosen to be approximately 150K. From figure 4a, G_{FS} is 0.62m℧ for an I_D of 20µA. V_{OUT}/V_G is calculated as (0.62m℧)(150K) = 93.

For a load current of 100mA, R_{LOAD} = 3.0V/100mA. Using figure 4b, V_{OUT}/V_G is calculated as (310m℧)(30Ω) = 9.3. The open-loop gain varies with load and is at its maximum during

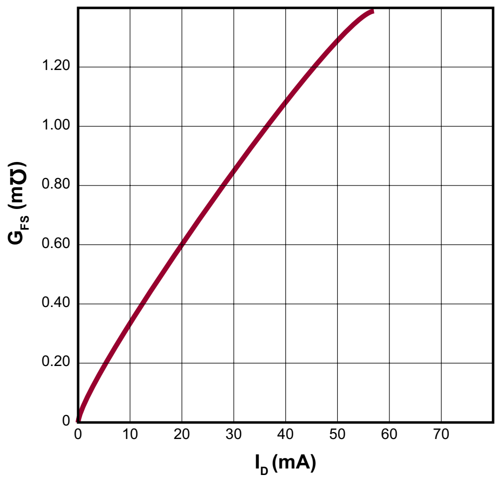


Figure 4a: G_{FS} vs. I_D at Low Currents

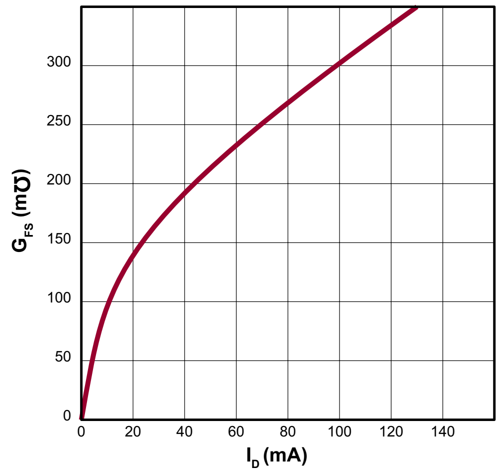


Figure 4b: G_{FS} vs. I_D at High Currents

the no load condition. The negative feedback, ß, is R_3 / (R_3 + R_4) and should be set less than or equal to 1/(V_{OUT}/V_G).

It is desirable to set ß <<1 / 93 since 1 / 93 is a typical value. R_3 and R_4 are chosen to be 500Ω and 150k respectively for a ß of 1/301, providing an adequate safety margin.

Calculations

The offset voltage, V_{OS}, input biasing current, I_b+ and I_b-, and tolerances of the external resistors will affect the output voltage. R_1 is used to adjust V_{OUT} to 3.0V. Figure 5 is an equivalent circuit showing V_{OS}, I_b+ , and I_b-.

To determine the range of R_1, the range of V_I needs to be determined under the worst case conditions. Using superposition, V_{OUT} is calculated as:

$$V_{OUT} = (V_{OS} + V_i)\left(\frac{R_4}{R_3} + 1\right) + (I_b+)\,R_4 + (I_b-)\,\frac{(R_1 R_2)}{(R_1 + R_2)}\left(\frac{R_4}{R_3} + 1\right)$$

The LM10 guarantees V_{OS} = 4.0mV max and I_b = 30nA max. (R_1 • R_2) / (R_1 + R_2) is set at 2K.
For minimum V_i:

$$3.0V = (V_i + 4mV)\left(\frac{157.5k}{475} + 1\right) + 30nA(157.5k) +$$

$$30nA\,(2k)\left(\frac{157.5k}{475} + 1\right)$$

$$3.0V = 3332.6V_i + 1.330V + 4.725mV + 19.95mV$$

$$V_{i(min)} = 4.947mV$$

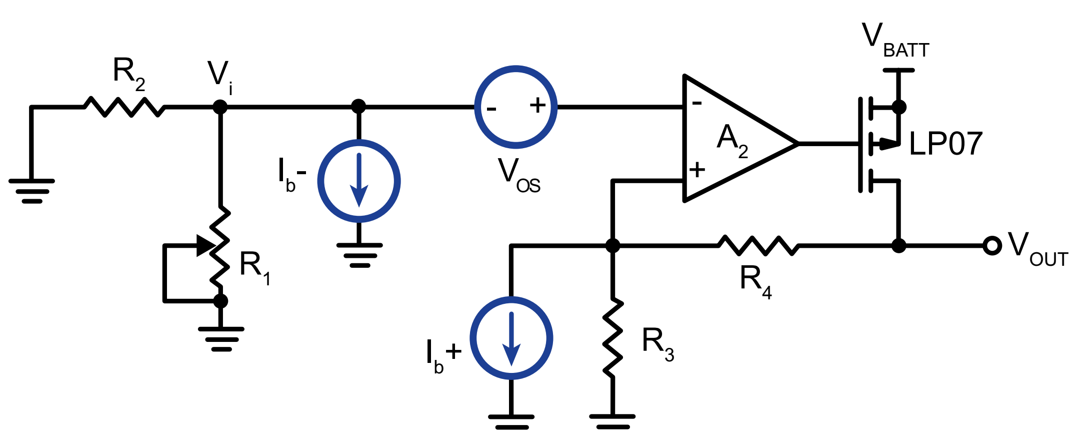


Figure 5: Offset Voltage and Input Biasing Current

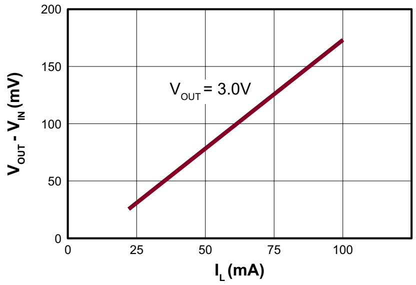


Figure 6: Dropout Voltage

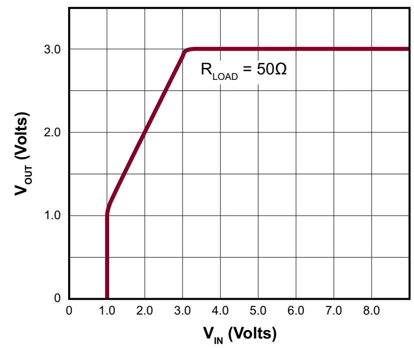


Figure 7: V_{OUT} vs V_{IN}

For maximum V_i:

$$3.0V = (V_i - 4mV)\left(\frac{142.5k}{525} + 1\right) - 30nA\,(142.5k) - 30nA\,(2k)\left(\frac{142.5k}{525} + 1\right)$$

$$3.0V = 272.4V_i - 1.090V - 4.275mV - 16.35mV$$

$$V_{i(max)} = 15.09mV$$

The range for R1 is:

$$V_i = \frac{R_1}{R_1 + R_2}(200mV)$$

$$R_1 = \frac{R_2}{39.40} \text{ to } \frac{R_2}{12.25}$$

Choosing R_1 to be a 2k potentiometer, R_2 = (2k)(12.25) = 24.5k. R_2 should be less than 24.5k so under the worst case conditions, R_1 would not operate at its maximum value of 2k. R_2 is chosen to be 22k. The range of R_1 is calculated as:

$$R_1 = 22k(0.95) / 39.4 \text{ to } 22k(1.05) / 12.25$$

$$R_1 = 531\Omega \text{ to } 1.89k\Omega$$

Measurements

Actual measurements were recorded and are shown on figures 6 and 7. Figure 6 shows the dropout voltage at different load currents. Figure 7 shows the output voltage regulation versus the decrease in battery voltage with a fixed load.

5.0V Regulators

The low dropout 3.0V regulator in figure 1 can be easily modified to a 5.0V or adjustable low dropout regulator by changing R_1 to a 5.0k potentiometer. Using a voltage controlled resistor for R_1 will allow for a programmable low dropout regulator.

Conclusion

Low dropout 3.0V linear voltage regulators are ideal for portable battery operated applications to help extend battery life. The low dropout voltage allows the battery powered equipment to operate at a lower battery voltage. In addition to the other advantages discussed, MOSFETs increase the efficiency of the circuit because of the current required to drive the gate is virtually zero as it is usually in the sub nanoampere area. Bipolars need base current and this is undesirable especially when battery energy is at a budget. LP07 is ideal for linear applications requiring high efficiency because of its low threshold voltage and low guaranteed on-resistances at 2V, 3V and 5V drives.

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