High Voltage Ramp Generator

Introduction

A low cost 500V high voltage ramp generator is shown in Figure 1. High voltage ramps are ideal for applications requiring a linear relationship between output voltage and time, e.g., high voltage sweeping, automatic test equipment and piezo electric drivers.

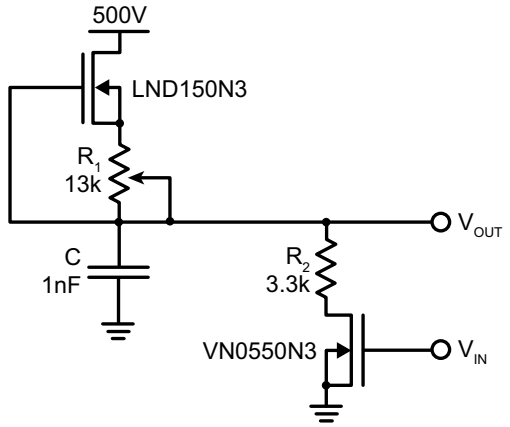


Figure 1

Circuit Description

The high voltage ramp generator shown in Figure 1 utilizes two Supertex high voltage DMOS transistors, the LND150N3 and the VN0550N3, two resistors, R_1 and R_2, and a capacitor C. R_1 is a trimpot resistor. The LND150N3 is a 500V ESD protected N-channel depletion-mode MOSFET and the VN0550N3 is a 500V N-channel enhancement-mode MOSFET. Both transistors are available in the TO-92 package.

The LND1 is configured as a constant current source charging a capacitor C. R_1 introduces negative feedback to regulate and set the desired constant current value. When the constant current source begins charging capacitor C, a voltage ramp is generated across the capacitor. The voltage ramp, V_{OUT}, is the voltage across the capacitor.

The VN0550 can be turned on with a TTL or CMOS control signal to reset the ramp voltage V_{OUT} by discharging the capacitor to ground through R_2. The VN0550 has a typical on-resistance of 45Ω at a 10V gate drive and 50Ω at a 5.0V gate drive. Resistor R_2 is calculated to limit the discharge current for the VN0550 to operate within its SOA rating.

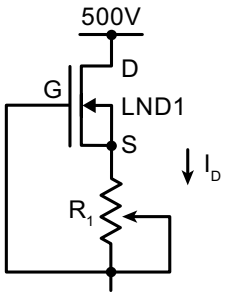
Calculations for Component Values

The ramp is designed to be 0.1V/µsec. Capacitor value C should be kept small to reduce charging and discharging a large amount of energy. The selection of C should be large enough so that output loads and stray capacitances will not introduce significant error. C is chosen to be 1.0 nF.

The charging characteristic for a capacitor is I = C (dv/dt).

$$I = 1.0\ nF \times 0.1\ V/\mu sec = 100\mu A.$$

Calculating R_1 for a 100 µA constant current source:



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2, \quad V_{GS} = -I_D R_1$$

$$= I_{DSS}\left(1 + \frac{I_D R_1}{V_{GS(OFF)}}\right)^2$$

Solving for R_1:

$$R_1 = \frac{V_{GS(OFF)}}{I_D}\left(\sqrt{\frac{I_D}{I_{DSS}}} - 1\right)$$

$V_{GS(OFF)}$ = pinch-off voltage. Measured value = -1.6V.
I_{DSS} = saturation current at V_{GS} = 0V.
Measured value = 3.0 mA.

Calculating for R_1 using the typical values:

$$R_1 = \frac{-1.6V}{100\mu A}\left(\sqrt{\frac{100\mu A}{3.0mA}} - 1\right) = 13.1k\Omega$$

R_1 should therefore be adjusted to approximately 13.1kΩ.

During power up and down, it is possible to have high transient voltages to the gate of the LND1. The LND1 internal ESD gate-to-source protection will protect the device against such transients.

The VN0550 performs the reset function by discharging capacitor C through resistor R_2. The VN0550's low output capacitance, (C_{OSS}) of 10pF max, minimizes additional parallel capacitance across capacitor C.

It is desirable to discharge V_{OUT} rapidly and as close to ground as possible. This can be accomplished with a low value R_2. However, care should be taken not exceed the SOA rating of the VN0550N3.

Maximum peak power for VN0550 in a TO-92 package is 3.0W.

Calculating for a minimum R_2:

$$
\begin{aligned}
P_{DISS} &= I_D \bullet V_{DS},\ V_{DS} = 500V - (I_D \bullet R_2) \\
I_{D(ON)}\ min &= 150mA, \\
P_{DISS} &= 3.0W \\
R_2 &= (1/I_D)(500V - P_{DISS}/I_D) \\
&= (1/150mA)(500V - 3.0W/150mA) \\
&= 3.2K\Omega
\end{aligned}
$$

R_2 is set to a standard resistor value of 3.3kΩ.

Figures 2 and 3 show two different input signals with their corresponding output voltage ramps. The ramp can be adjusted by varying R_1.

Conclusion

The LND1 is ideally suited for high voltage, low constant current source applications. High voltage ramp generators, high voltage triangular waveform generators, high voltage references, biasing circuitry and active loads for discrete high voltage amplifiers are some examples.

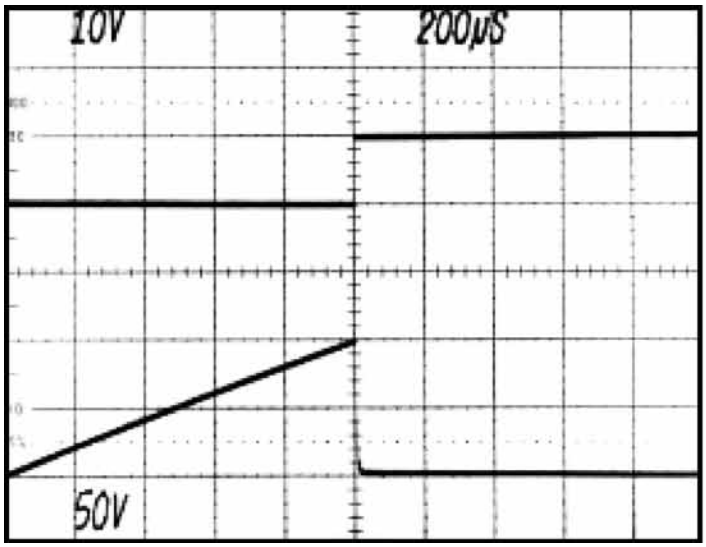


Figure 2

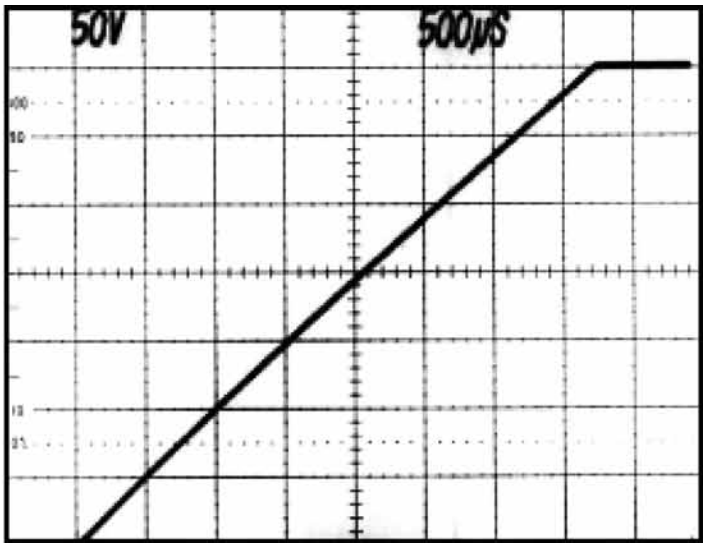


Figure 3

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