Low-Threshold TN/TP Series MOSFETs: Structure, Performance and Applications

Introduction

Since an increasing amount of attention is being focused on system interface from low-level logic, the need for higher current and/or low on-resistance at drive levels of only 3.0 - 5.0V has become a major concern. Supertex has always known of the importance of the gate drive consideration and has been offering N-channel low-threshold devices with threshold voltages of 2.4 and 1.6V for many years. Additionally, standard and low-threshold versions of P-channel DMOS devices are available. To understand the reasons that low-threshold processing requires very specialized techniques, one needs to understand the DMOS structure.

DMOS Structure

Most double-diffused MOS (DMOS) structures have very similar cross-section characteristics, as shown in Figure 1. For conduction to occur, a channel of electrons is needed between the gate and the source. This potential produces an inversion layer called the channel. The depth of this layer is the limiting factor in allowing current flow between the drain and source terminal. The greater the voltage applied, the deeper the induced channel; resulting in more current flow. The voltage needed to invert the channel region is called the threshold voltage $V_{GS(th)}$. However, when examining most manufacturers' databooks, one finds $V_{GS(th)}$ defined as the voltage needed to produce a specified drain current (I_D). This differs from the theoretical definition of knowing when a channel is produced, which is of little interest to MOSFET users. Comparing $V_{GS(th)}$ at the same I_D simplifies the analysis of databook parametric guarantees, allowing the designer to compare the product to actual needs.

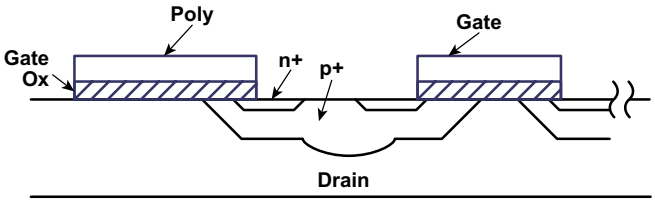

Figure 1: Double Diffused MOS (DMOS)

The control of the threshold voltage is dependent on many factors, such as dopant concentration, gate-to-silicon work function and surface change. The greater the body dopant concentration, the larger the applied voltage needed to produce a channel, which translates to a higher threshold voltage. One method of reducing threshold voltage is to reduce the body dopant concentration until the required $V_{GS(th)}$ is met. This technique by itself is dangerous because it degrades other device parameters. The first and most important of these is drain-source breakdown (BV_{DSS}), which is a result of certain conditions, most commonly punch-through. Punch-through is defined as the drain voltage needed to create an electric field connecting the drain and source, as shown in Figure 2, at voltages less than the actual BV_{DSS} rating.

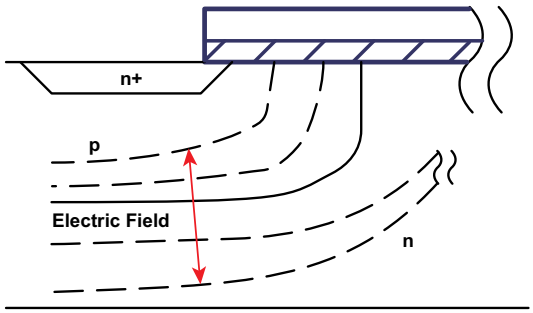

Figure 2: Electric Field Connecting Drain and Source

The susceptibility to punch-through increases dramatically as the body dopant concentration is lowered. There is an optimum body dopant level that is needed in order to stay away from the punch-through mechanism, but this concentration is too high for low thresholds. This is one of the reasons why P-channel devices typically have higher thresholds, because the optimum body dosage is higher than N-channel FETs.

Another technique, used by some manufacturers, is to lower threshold by reducing the gate oxide thickness. Again, there are trade-offs using this method: (1) The input capacitance increases which will effect the switching speed efficiency and (2) the maximum gate voltage rating is decreased, making it more susceptible to input voltage spikes.

Supertex has developed a proprietary technique to successfully lower threshold voltage without these major trade-offs. This method mainly depends on modifying the diffusion profile and altering the charge distribution to produce low-threshold N- and P-channel devices. This process, which makes use of Supertex's interdigitated design structure, allows typical thresholds of 1.1V for N-channel and 1.8V for P-channel, DMOS devices.

Part	IRF520			VN2210N3			Units
Parameter	Min	Max	Conditions	Min	Max	Conditions	
$V_{GS(th)}$ - Gate threshold voltage	2.0	4.0	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	0.8	2.4	$V_{DS} = V_{GS}$, $I_D = 10mA$	V
$I_{D(ON)}$ - On-state drain current	8.0	-	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ max $V_{GS} = 10V$	8.0	-	$V_{DS} = 25V$, $V_{GS} = 10V$	A
				3.0	-	$V_{DS} = 25V$, $V_{GS} = 5.0V$	
$R_{DS(ON)}$ - Drain-to-source on-resistance	-	0.3	$V_{GS} = 10V$, $I_D = 4.0A$	-	0.35	$V_{GS} = 10V$, $I_D = 4.0A$	Ω
					0.50	$V_{GS} = 5.0V$, $I_D = 1.0A$	

Table 1. Comparison between MOSFET and standard threshold Supertex device

An added benefit of Supertex's design is the lower input capacitance achieved by the interdigitated geometry, rather than the more conventional closed cell approach. Less charge is needed to control the device input. Therefore, it can be concluded that a lower threshold device will start conducting earlier for a given gate drive and allow control of larger drain current than a higher threshold device.

The availability of such low-threshold DMOS devices insures the performance needed to be driven by low level logic systems, in which the maximum voltage available is only 3-5V.

Performance Advantages

With the first device shipped in 1982, Supertex was the pioneer in low-threshold DMOS FET technology and still maintains a performance edge over other manufacturers. Supertex currently supplies the lowest threshold MOSFETs in the industry. A threshold voltage of 1.0V for N-channel as well as for P-channel clearly supports this claim.

Supertex measures threshold voltages at I_D = 1.0mA, 2.5mA, and 10mA for small, medium and large-sized devices, respectively. Although some manufacturers use test conditions as low as I_D = 250µA for large devices, Supertex devices, in comparison, still have lower values of threshold voltages at higher values of I_D. See Table 1 for a comparison between a popular MOSFET and a standard-threshold Supertex device.

A true comparison can be made by normalizing the value of the I_D test condition. The threshold voltage for VN2210N3 will be lower than 2.4V (max) when it is tested at I_D = 250µA. Supertex's test conditions therefore portray a realistic picture of the device's capabilities at low V_{GS} conditions.

The threshold voltage is an important indicator of performance at low VGS conditions because a device that starts conducting at a very low bias will exhibit good characteristics under such conditions. In fact, $R_{DS(ON)}$ (max) and $I_{D(ON)}$ (min) at low V_{GS} conditions are much more important than just the threshold voltage value because quiescent gate voltage conditions are usually at least a few volts above the $V_{GS(th)}$ value. Figure 3 shows the transfer characteristics of a standard-threshold and a low-threshold device. For example, if the drain current requirement is 100mA, TN2524N8 will typically need V_{GS} = 1.75V and VN2224N3 will require 2.4V to achieve this value. In case a 2.4V drive is not available, as in many applications, a VN2224N3 will be incapable of functioning in the circuit. In spite of the TN2524N3 die being 3.6 times smaller than the VN2224, the TN2524N8 performance is far superior at low gate to source voltages.

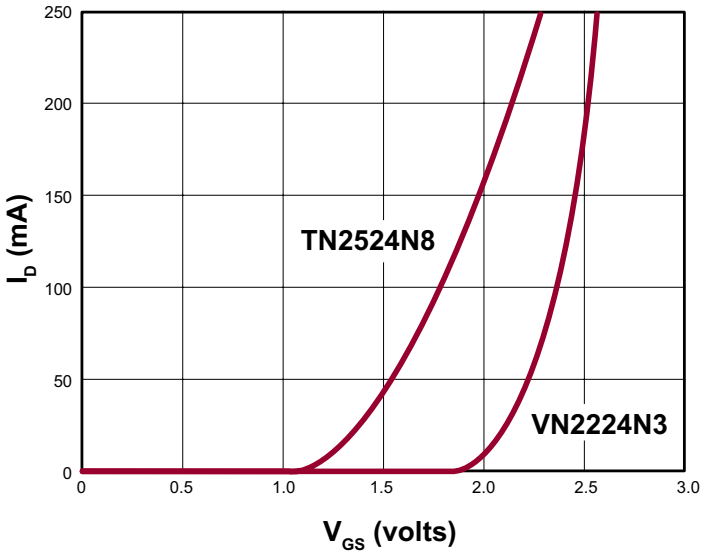

Figure 3: Typical Transfer Characteristics

When confronted by low gate drive voltage, a designer basically has two choices:

Approach 1:

Use a large industry-standard-threshold device to obtain the required low $R_{DS(ON)}$, maximum and $I_{D(ON)}$, minimum values. $I_{D(ON)}$ can be obtained from the transfer characteristics and $R_{DS(ON)}$ values will be read off the typical saturation or output characteristics.

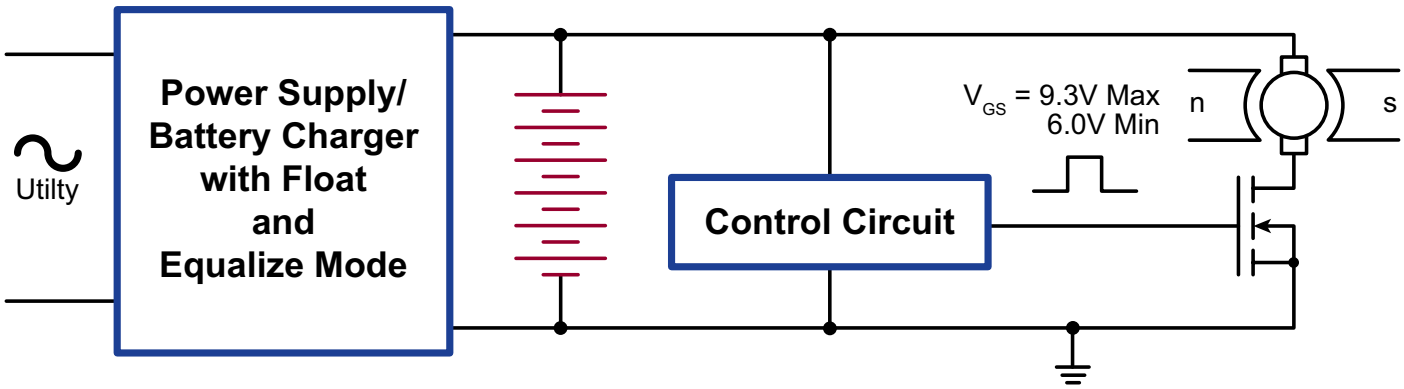

Figure 4: Motor of a Fluid Injection Pump

Approach 2:

Compared to the device used in Approach 1, use a relatively small (die size), low-threshold device to achieve the desired $I_{D(ON)}$ and $R_{DS(ON)}$ at the given minimum gate-to-source voltage.

Comparison of Approach 1 and 2

1. Large die always have larger parasitic capacitance and consequently slower switching speeds. This could pose a restriction in many applications, where limited gate drive charging current is available.
2. Large die must be accommodated in large packages, and this may result in unnecessary waste of board space. For example, the total volume occupied by a TO-220 package including stand off could be 8 to 10 times more than a TO-92 package.
3. A judicious choice using smaller die in a smaller package can result in considerable cost savings. With more silicon and several times the raw material content for packaging, a low-threshold TO-92 will definitely be a much more cost-effective alternative.

Supertex publishes $R_{DS(ON)}$, maximum, and $I_{D(ON)}$ minimum, specifications at V_{GS} = 5.0V (see Table 1). This data is very useful to a designer because it is always desirable to rely on guaranteed values instead of typical curves. Typical curves are based on a high statistical probability of the majority of devices closely meeting values on the curves. They do not 100% guarantee performance of all devices. Manufacturing tolerances and some variations from one fabrication lot to another are likely to cause lower than expected values of these parameters. Depending entirely on curves tends to be risky for production runs even if prototypes built earlier perform satisfactorily.

The combined effect of low-threshold voltage and low-input capacitance is ease of drive, which is a key consideration in most circuits employing MOSFETs. What better trait can a designer expect than a small amount of charge controlling high voltages and large currents? These low-threshold FETs from Supertex are ideally suited to interface low-voltage logic to the outside world.

Applications

Low-threshold MOSFETs play a key role in circuit design whenever there is a low gate-to-source voltage situation. Conventional devices are often very inefficient and sometimes unusable in some applications as follows:

- Handheld, battery-operated equipment requiring satisfactory operation at low/end-of-discharge voltages. This is necessary for complete utilization of battery energy. Inadequate turn-on of a FET can cause two problems: A) loss of control signal or data; or B) loss of power due to resistive losses. Supertex TN/TP series devices are being used for a variety of data acquisition and remote-control applications.
- Medical equipment with battery backup is another popular application. Figure 4 shows the motor of a fluid injection pump powered by the utility supply and backed by a NiCad battery. The V_{GS} = 6.0V condition demands careful attention, because the $R_{DS(ON)}$ has to be low in order to ensure a low drain to source voltage drop. A large voltage drop can: A) affect motor performance, and B) cause high I^2R losses, reducing system efficiency and battery back-up time.
- Solid-state relays utilize optically-isolated drive schemes for isolation purposes. Figure 5 shows a commonly-used photovoltaic drive scheme. Usually a low voltage is available to turn on the FET to meet the

relay's assured $R_{DS(ON)}$ specifications. Precautions are taken to avoid excessive drive since the charge applied during turn-on must be quickly discharged during turn-off. Turn-off circuitry is not shown in this simplified schematic.

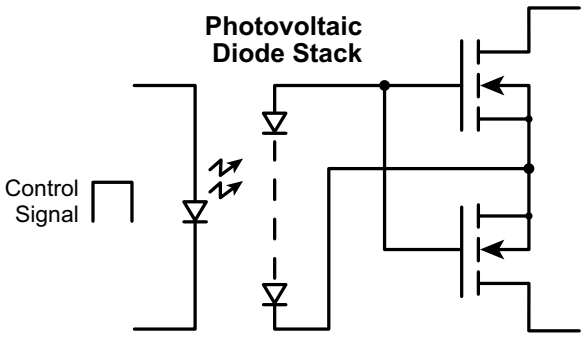

Figure 5: Photovoltaic Drive Scheme

Figure 6 shows a simple charge pump converting 5.0 to 12VDC. The key parameter for efficient functioning of this circuit is $R_{DS(ON)}$ at V_{GS} = 5.0V.

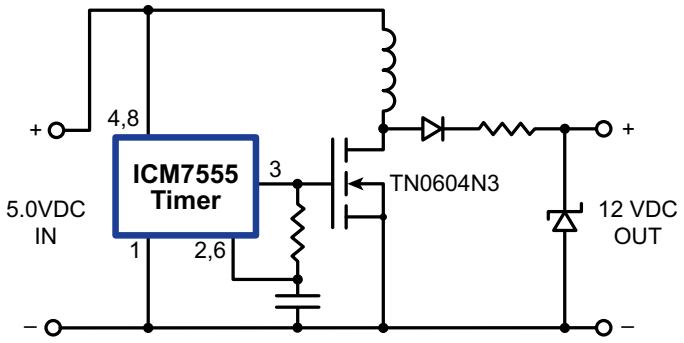

Figure 6: Charge Pump Converting 5.0 to 12VDC

Advances in low-threshold MOSFET technology offer several useful choices to a designer. Circuit designs for many applications are simplified and use of components is minimized. Consequently, system complexity is reduced and reliability enhanced. All these benefits, combined with the cost-effectiveness of the devices, make the low-threshold FETs an excellent choice.

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com